Preliminary

OKI Semiconductor

This version: Oct. 1998

MSM7662

NTSC/PAL Digital Video Decoder

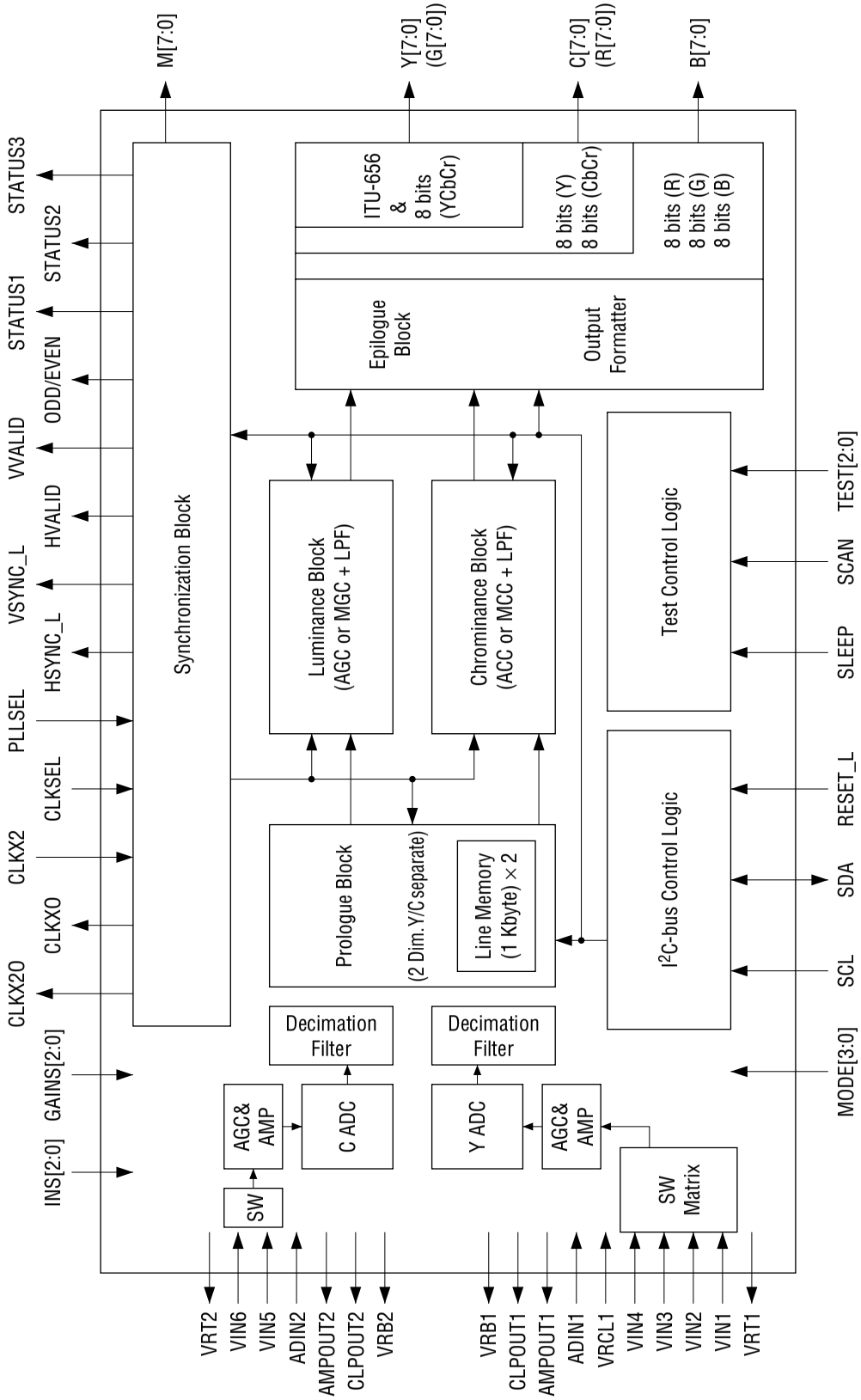
GENERAL DESCRIPTION

The MSM7662 is an LSI device that decodes NTSC or PAL analog video signals into YCbCr and RGB digital data based on ITU-RBT.601.
The device has built-in two channels of A/D converters and can accept composite video and S video signals for the input video signals. Composite video signals are converted to YCbCr and RGB digital data via the 2-dimensional Y/C separation circuit with an adaptive filter.
Analog video signals can be sampled by a clock at the pixel frequency or at twice the pixel frequency. A decimation filter is built-in for sampling at twice the pixel frequency.
Input signals are synchronized internally and high-speed locking for color burst is possible. Because a FIFO buffer is built into the output format circuit, jitter-free output can be obtained even for non-standard signals.

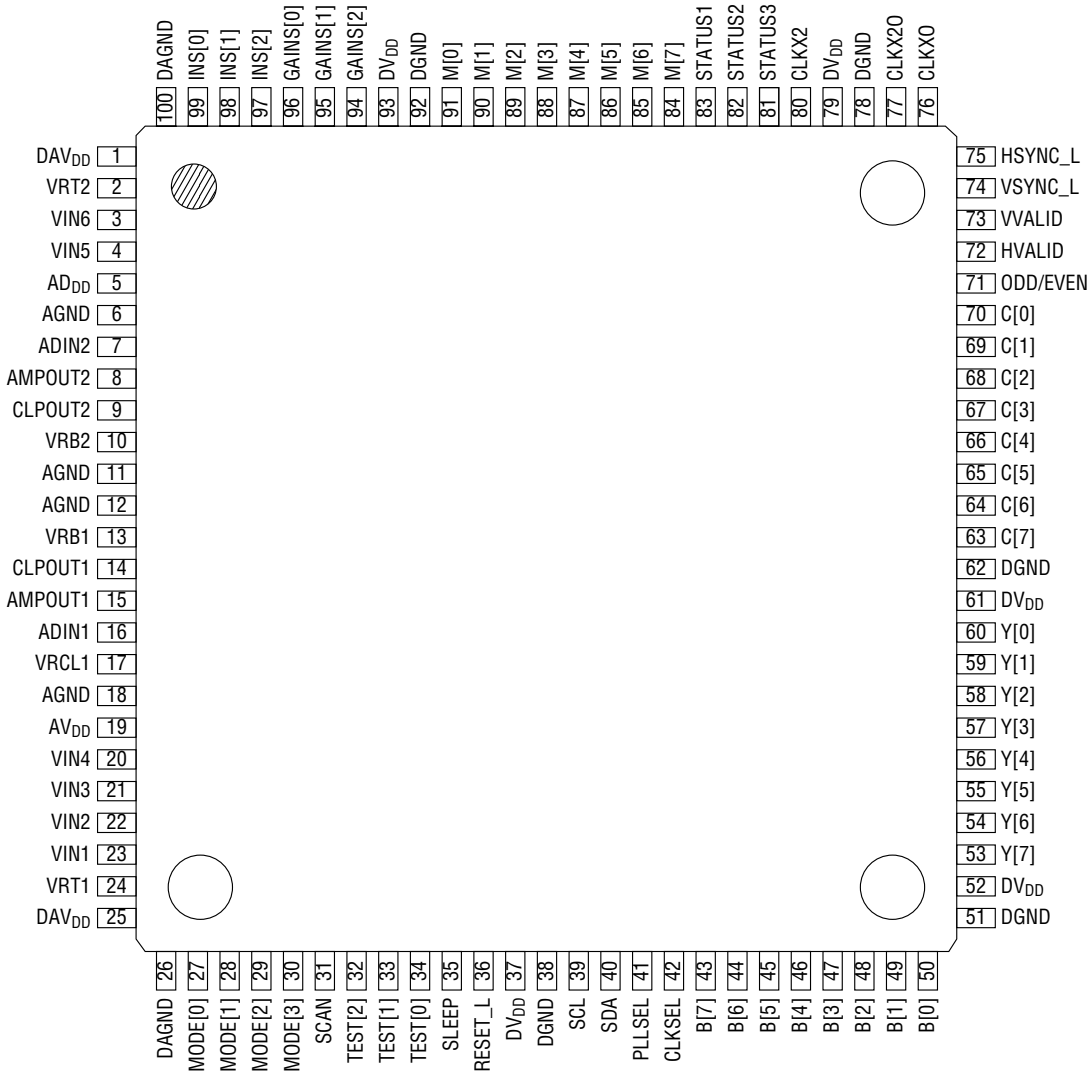
FEATURES (• new feature not found on MSM7661)

◦ Input analog signal
  NTSC/PAL composite video signal or S-video signal
• 5 composite, 2 S-video analog inputs (switchable)
• Built-in clamp circuits and video amps
• Built-in 8-bit A/D converters (2 channels; sampling frequency: 40 MHz)
• 4 selectable output interfaces
  ITU-RBT.656 (conditional), 8-bit (YCbCr), 8-bit (Y) + 8-bit (CbCr)
  YCbCr = 4 : 2 : 2, YCbCr = 4 : 1 : 1 (limit)
  24-bit RGB RGB = 4 : 4 : 4
◦ 2-dimensional Y/C separation using adaptive comb filter (this filter is bypassed for S-video signal input)
  NTSC format: 3 lines or 2 lines, PAL format: 2 lines (3 virtual lines)
• Selectable input signal synchronization
  4 synchronization modes: FIFO-1, FIFO-2, FM-1, FM-2 (FIFO-1 is normally selected)
  (FIFO-1 and FIFO-2 use the internal FIFO, FM-1 and FM-2 use external field memory)
◦ Compatible pixel frequencies
  13.5 MHz (ITU-RBT.601), 12.27 MHz (NTSC Square Pixel)
  14.31818 MHz (NTSC 4fsc), 14.45 MHz (PAL Square Pixel)
• Built-in AGC/ACC circuits, compatible with a wide range of input levels
  Input level range: –8 dB to +3.5 dB
  Switchable between AGC/MGC (fixed gain) and ACC/MCC (fixed gain)
◦ Decimation filter built into input stage, allows easy configuration of filter prior to A/D converter
◦ Automatic NTSC/PAL recognition (only for ITU-RBT.601)
◦ Sleep mode
◦ Multiplex signal recognition (closed caption)
  During vertical blanking interval, data is output as 8-bit data.
◦ I^2C-bus interface
◦ 3.3 V single power supply (I/O 5 V tolerance)
• Package:
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product name: MSM7662TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	DAV_{DD}	—	Digital power supply in A/D converter
2	VRT2	O	A/D converter reference voltage (high side) for chroma signal
3	VIN6	I	Chroma signal input pin (leave open or connect to AGND when not used)
4	VIN5	I	Chroma signal input pin (leave open or connect to AGND when not used)
5	AV_{DD}	—	Analog power supply
6	AGND	—	Analog ground
7	ADIN2	I	A/D converter input pin for chroma signal
8	AMPOUT2	O	Chroma signal amp output
9	CLPOUT2	O	Chroma signal clamp voltage output
10	VRB2	O	A/D converter reference voltage (low side) for chroma signal
11	AGND	—	Analog ground
12	AGND	—	Analog ground
13	VRB1	I	A/D converter reference voltage (low side) for composite/luminance signal
14	CLPOUT1	O	Composite/luminance signal clamp voltage output
15	AMPOUT1	O	Composite/luminance signal amp output
16	ADIN1	I	A/D converter input pin for composite/luminance signal
17	VRCL1	I	Luminance signal clamp voltate input
18	AGND	—	Analog ground
19	AV_{DD}	—	Analog power supply
20	VIN4	I	Composite/luminance signal input (leave open or connect to AGND when not used)
21	VIN3	I	Composite/luminance signal input (leave open or connect to AGND when not used)
22	VIN2	I	Composite/luminance signal input (leave open or connect to AGND when not used)
23	VIN1	I	Composite/luminance signal input (leave open or connect to AGND when not used)
24	VRT1	O	A/D converter reference voltage (high side) for composite/luminance signal
25	DAV_{DD}	—	Digital power supply in A/D converter
26	DAGND	—	Digital ground in A/D converter
27 to 30	MODE[3:0]	I	Mode selection pins (pulled-down by internal resistors) MODE[3:2] Output mode selection 00: ITU-RBT.656 (with SAV, EAV, blank processing) 01: ITU-RBT.656 (no SAV, EAV, blank processing) 10: ITU-RBT.601 11: RGB MODE[1] 0: NTSC 1: PAL MODE[0] 0: ITU-RBT.601 1: Square Pixel If an ITU-R.601 signal is input while registers are set to automatic NSTC/PAL recognition, NTSC/PAL will be automatically recognized regardless of the MODE1 setting.

PIN DESCRIPTIONS (continued)

Pin	Symbol	Type	Description
31	SCAN	I	Test input. Normally fixed at "0" (pulled down by internal resistor).
32	TEST[2]	I	Test input. Normally fixed at "0" (pulled down by internal resistor).
33	TEST[1]	I	Test input. Normally fixed at "0" (pulled down by internal resistor).
34	TEST[0]	I	Test input. Normally fixed at "0" (pulled down by internal resistor).
35	SLEEP	I	0: normal operation, 1: sleep operation
36	RESET_L	I	Reset input pin (active "L")
37	DV_{DD}	—	Digital power supply
38	DGND	—	Digital ground
39	SCL	I	I^2C-bus clock input
40	SDA	I/O	I^2C-bus data I/O pin
41	PLLSEL	I	Internal/external sync switching pin (pulled down by internal resistor). 0: Internal sync mode, 1: External sync mode; use external PLL
42	CLKSEL	I	Clock select input pin (pulled down by internal resistor). "L": double-speed 27 MHz, "H": normal clock 13.5 MHz
43 to 50	B[7:0]	I/O	B data output during RGB mode B[7]: MSB, B[0]: LSB
51	DGND	—	Digital ground
52	DV_{DD}	—	Digital power supply
53 to 60	Y[7:0]	O	ITU-RBT.656 data output during ITU-RBT.656 output mode ITU-RBT.601 luminance data output during ITU-RBT.601 output mode G data output during RGB mode, Y[7]: MSB, Y[0]: LSB
61	DV_{DD}	—	Digital power supply
62	DGND	—	Digital ground
63 to 70	C[7:0]	I/O	Chroma data output during ITU-RBT.601 output mode R data output during RGB mode, C[7]: MSB, C[0]: LSB
71	ODD/EVEN	O	Field display output If field is odd, "H" is output
72	HVALID	O	Horizontal valid pixel timing output pin
73	VVALID	O	Vertical valid line timing output pin
74	VSYNC_L	O	V sync output pin
75	HSYNC_L	O	H sync output pin
76	CLKXO	O	Pixel clock output
77	CLKX2O	O	System clock output
78	DGND	—	Digital ground
79	DV_{DD}	—	Digital power supply
80	CLKX2	I	System clock input
81	STATUS[3]	O	Default is internal FIFO overflow detection (TV, VTR mode switching guide) 0: non-detection, 1: detection CSYNC output (selected by register) When PLLSEL external sync mode is selected, HSYNC output

PIN DESCRIPTIONS (continued)

Pin	Symbol	Type	Description
82	STATUS[2]	O	Default is NTSC-PAL recognition 0: NTSC, 1: PAL HLOCK sync detection display output (selected by register) 0: non-detection, 1: detection
83	STATUS[1]	O	VBI interval multiplex signal detection output 0: non-detection, 1: detection
84	M[7]	I/O	Field memory control signal; RE output
85	M[6]	I/O	Field memory control signal; WE output
86	M[5]	I/O	Field memory control signal; RSTR output
87	M[4]	I/O	Field memory control signal; RSTW output
88	M[3]	I/O	Test output pin, normally "L" output
89	M[2]	I/O	Slave address select "L": 1000001X "H": 1000011X (no internal pull-up or pull-down resistor)
90	M[1]	I/O	Pin for setting by either external pin or internal register in order to select analog section gain value and video signal input pin. "L": external pin setting "H": internal register setting (no internal pull-up or pull-down resistor)
91	M[0]	I/O	Test I/O pin, normally fixed at "H" (no internal pull-up or pull-down resistor)
92	DGND	—	Digital ground
93	DV_{DD}	—	Digital power supply
94 to 96	GAINS[2:0]	I	Inputs for amp gain switch setting during external setting mode (pulled down by internal resistors)
97 to 99	INS[2:0]	I	Inputs for signal input pin switch setting during external setting (pulled down by internal resistors)
100	DAGND	—	Digital ground in A/D converter

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +4.5	V
Input Voltage	V_I	V_{DD} = 3.3 V	–0.3 to +5.5	V
Power Consumption	P_W	—	1	W
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	3.0	3.3	3.6	V
Power Supply Voltage	GND	Ta = 25°C	—	0	—	V
Digital "H" Level Input Voltage	V_{IH1}	—	2.2	—	V_{DD}	V
	V_{IH2} (*1)	—	$0.8 \times V_{DD}$	—	V_{DD}	V
Digital "L" Level Input Voltage	V_{IL}	—	0	—	0.8	V
Analog Video Signal Input	V_{AIN}	SYNC tip to white peak level	0.8	—	1.1	V_{P-P}
Operating Temperature	Ta	—	0	—	70	°C

*1: CLKX2, SDA

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = 0 to 70°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Output Voltage	V_{OH}	I_{OH} = –4 mA (*1)	0.7 × V_{DD}	—	V_{DD}	V
		I_{OH} = –6 mA (*2)				
"L" Level Output Voltage	V_{OL}	I_{OL}= 4 mA (*1)	0	—	0.8	V
		I_{OL}= 6 mA (*2)				
Input Leakage Current	I_{LI}	V_I = GND to V_{DD}	–10	—	+10	µA
		R_{pull_down} = 50 kΩ (*3)	–250	—	–20	µA
Output Leakage Current	I_{LO}	V_I = GND to V_{DD}	–10	—	+10	µA
SDA Output Voltage	$SDAV_L$	—	0	—	0.4	V
SDA Output Current	$SDAI_O$	—	3	—	—	mA

*1: HSYNC_L, VSYNC_L, SYSSEL, C[7:0], B[7:0], ODD, VVALID, HVALID, CLKXO, HSY
*2: Y[7:0], CLKX2O
*3: MODE[3:0], TE, TEST1, T0, T1, PLLSEL, CLKSEL, M[3:0], ATEST[3:1], INS[3:1]

DC Characteristics (Analog Unit)

(Ta = 0 to 70°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AMPOUT Output Voltage	V_{OAMP}	R_O = 330 Ω	0.2	—	2.6	V
CLPOUT Output Voltage	V_{OCLP}	R_O = 5 kΩ	0.2	—	1.6	V
VRT Output Voltage	V_{RT}	—	2.05	2.3	2.4	V
VRB Output Voltage	V_{RB}	—	0.15	0.3	0.4	V
ADIN	V_{IADIN}	—	V_{RB}	—	V_{RT}	V
VIN	V_{IVIN}	Capacitive coupling	0.4	—	1.3	V_{P-P}
Input Current	I_{IVIN}	V_I = 1.5 V	60	100	200	µA

DC Characteristics

(Ta = 0 to 70°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current (Operating)	I_{D1}	AD1 on AD1 off CLKX2 = 27 MHz	150	210	TBD	mA
Power Supply Current (Operating)	I_{D2}	AD1 on AD2 on CLKX2 = 27 MHz	190	240	TBD	mA
Power Supply Current (Sleep)	I_{DS}	V_I = 1.5 V	0.2	1	5	mA

AC Characteristics (Single Speed Mode)

(Ta = 0 to 70°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Time	t_{CLKX1}	ITU-RS601	—	74.07	—	ns
		NTSC 4fsc	—	69.84	—	ns
		NTSC Square Pixel	—	81.5	—	ns
		PAL Square Pixel	—	67.8	—	ns
CLKX1 Duty	t_{D_D1}	CLKSEL : H	40		60	%
Output Data Delay Time 1 (*)	t_{OD11}	—	7	—	28	ns
Output Data Delay Time 2 (*)	t_{OD12}	—	7	—	35	ns
Output Clock Delay Time (*) (CLKX2-CLKXO)	t_{CXD11}	CLKSEL : H	3	—	22	ns
Output Clock Delay Time (*) (CLKX2-CLKX2O)	t_{CXD12}	CLKSEL : H	3	—	16	ns
SCL Clock Cycle Time	t_{C_SC1}	R_{pull_up} = 4.7 kΩ	200	—	—	ns
SCL Clock Duty	t_{D_SC1}	—	—	50	—	%
SCL Low Level Cycle	t_{L_SC1}	R_{pull_up} = 4.7 kΩ	100	—	—	ns

(*) Output load: 15 pF

AC Characteristics (Double Speed Mode)

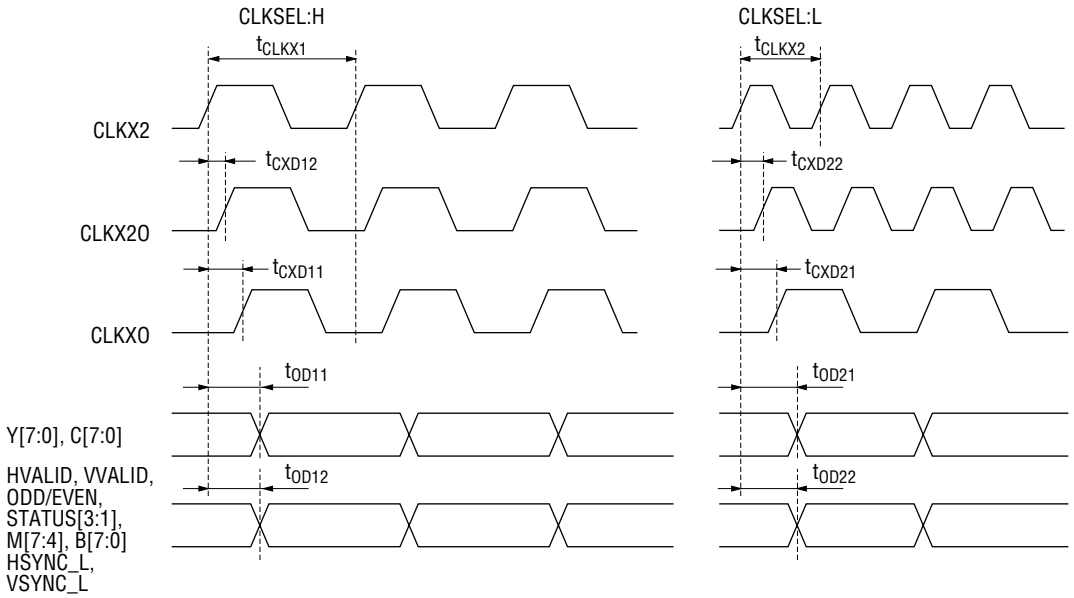
(Ta = 0 to 70°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Time	t_{CLKX2}	ITU-RS601	—	37.05	—	ns
		NTSC 4fsc	—	34.9	—	ns
		NTSC Square Pixel	—	40.75	—	ns
		PAL Square Pixel	—	33.9	—	ns
CLKX2 Duty	t_{D_D2}	—	45	—	55	%
Output Data Delay Time 1 (*)	t_{OD21}	CLKSEL : L	8	—	28	ns
Output Data Delay Time 2 (*)	t_{OD22}	CLKSEL : L	8	—	34	ns
Output Clock Delay Time (*) (CLKX2-CLKXO)	t_{CXD21}	CLKSEL : L	6	—	22	ns
Output Clock Delay Time (*) (CLKX2-CLKX2O)	t_{CXD22}	CLKSEL : L	5	—	16	ns
SCL Clock Cycle Time	t_{C_SCL}	R_{pull_up} = 4.7 kΩ	200	—	—	ns
SCL Clock Duty	t_{D_SCL}	—	—	50	—	%
SCL Low Level Cycle	t_{L_SCL}	R_{pull_up} = 4.7 kΩ	100	—	—	ns

(*) Output load: 15 pF

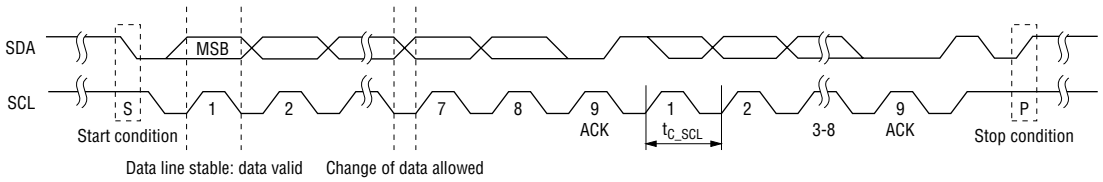
INPUT AND OUTPUT TIMING

Clock and Output Timing



I²C-bus Interface Input/Output Timing

The basic input/output timing of the I²C-bus is indicated below.



FUNCTIONAL DESCRIPTION

Analog Unit

1) Analog input select: Compatible with composite video signals and S-video signals. Input selection can be switched by register control via the I²C-bus or by external pins. (See the below chart for pin combinations.)
2) Clamp function: An analog clamp and a digital pulse clamp can be used.
Analog clamp (HSY = 1)*
Analog clamp → HSY clamp (digital clamp)
HSY clamp (digital clamp)
Only the HSY clamp can be set as the pedestal clamp.
3) AGC amp: The AGC function operates depending upon the input level.
Manual gain setting is also possible. This AGC function operates at 2 stages, the analog unit and digital unit. Digital decoded data is output in conformance with ITU-RBT.601.
4) A/D converter: Two internal 8-bit A/D converters sample at twice the pixel frequency. (Sampling at the pixel frequency is possible by changing the register setting.)

List of Analog Input Conditions

Input Signal	@Control Pin	Input Pin						ADC Selection	
	INS[2:0]	VIN1	VIN2	VIN3	VIN4	VIN5	VIN6	ON	OFF
Composite Input*	[000]	Composite						ON	OFF
Composite Input	[001]		Composite					ON	OFF
Composite Input	[010]			Composite				ON	OFF
Composite Input	[011]				Composite			ON	OFF
Composite Input	[100]					Composite		ON	OFF
S-video Input	[101]	Luminance				Chroma		ON	ON
S-video Input	[110]		Luminance				Chroma	ON	ON
All inputs Off	[111]	OFF (Sleep)						OFF	OFF

Blank spaces: non-selectable *: register default setting after LSI reset
@: These pin settings are valid during external mode setting. In the internal register mode, the register contents will be changed.

Manual Gain Control (analog AMP gain)

Gain Setting Pins GAINS[2:0]	Set Gain Value Typ. Value (multiplication factor)
[000]	1.0
[001]	1.35
[010]	1.75
[011]	2.3
[100]	3.0
[101]	3.8
[110]	5.0
[111]	2.0

Decoder Unit

1. Prologue Block

The prologue block inputs data and performs Y/C separation.
Data can be input at either the pixel frequency (ITU-R: 13.5 MHz) or at twice the pixel frequency (ITU-R: 27 MHz). If input at twice the pixel frequency, data is processed after passing through a decimator circuit to convert it to the pixel frequency. The decimator circuit may be bypassed by changing the register setting, regardless of whether data is input at the normal pixel frequency or at twice the pixel frequency.

If a composite signal (CVBS) is input, the default setting performs Y/C separation using a 2-dimensional adaptive comb filter.
The following operating modes can be selected via the I²C-bus. Default settings are indicated by an asterisk (*). The default state is selected at reset.

1) Video input mode selection
   Composite video input *
   S-video input
2) Video input mode selection
   NTSC/PAL auto-select* (only for ITU-R.601)
   Dependent upon operating mode selected

   When ITU-R.601 is selected, the video input mode is automatically set depending upon the number of lines per field.

3) Operating mode selection

NTSC ITU-R.601	13.5 MHz*
NTSC Square Pixel	12.27 MHz
NTSC 4fsc	14.31818 MHz
PAL ITU-R.601	13.5 MHz
PAL Square Pixel	14.75 MHz

4) Decimator circuit pass/bypass selection
   Pass through decimator circuit*
   Bypass decimator circuit
5) Y/C separation mode selection
   Use adaptive comb filter*
   Use non-adaptive comb filter
   Do not use comb filter (use trap filter)

The adaptive comb filter makes the correlation between up to 3 consecutive lines (only 2 lines in the case of a PAL signal). If there is correlation, Y/C separation is performed by the comb filter according to the format of correlation.
The non-adaptive comb filter performs Y/C separation by removing the luminance component based on the average of preceding and following lines (when there is correlation between 3 lines).
When a comb filter is not used, Y/C separation is performed by a trap filter.

If an S-video signal is input, these Y/C separation circuits are bypassed.

The functions of this block only operate when lines are valid as image information. During the V blanking interval, CVBS signals are not processed.

2. Luminance Block

The luminance block removes synchronous signals from signals containing luminance components after Y/C separation. The signals are compensated and then output as luminance signals. Two modes of gain control functions can be selected for the luminance signal output level: AGC (Auto Gain Control) and MGC + Pedestal Clamp.

In the AGC mode, luminance level amplification is determined by comparing the SYNC depth with a reference value. The default is 40IRE and can be changed by the register setting. The input has a sync chip clamp.
In the MGC + Pedestal Clamp mode, the signal output level is clamped to the pedestal level of the input. Signal amplification and black level can be changed from the clamped position by register settings.
This block can select the follwing operating modes.

1) Selection of prefilter and sharp filter usage
   Do not use*
   Use
   These filters are used to enhance the edges of luminance component signals.
2) Selection of aperture bandpass filter coefficient
   Middle range*
   High range
3) Coring range selection
   Off*
   ±4LBS
   ±5LBS
   ±7LBS
4) Aperture weighting coefficient selection
   0*
   0.25
   0.75
   1.5
   Both coring and aperture compensation processes perform contour compensation.
5) Selection of pixel position compensating circuit usage
   Use*
   Do not use
6) AGC loop filter time constant selection

Slow	coefficient value	1/1024n
Medium		1/64n*
Fast		1/n
Fixed		0

   Fixed: manual gain setting is possible

7) Parameter for fine adjustment of AGC sync depth
8) Parameter for fine adjustment of sync removal level
   The black level is adjusted. The default setting outputs the pedestal position as a black level (=16).
9) Pedestal clamp selection
   Do not use pedestal clamp*
   Use pedestal clamp (at this time, AGC does not operate, MGC operates)

3. Chrominance Block

This block processes the chroma signals.
The following operating modes can be selected.

1) Selection of color bandpass filter usage
   Do not use*
   Use
2) ACC loop filter time constant selection

Slow	coefficient value	1/1024m
Medium		1/64m*
Fast		1/m
Fixed		0

   Fixed: manual gain setting is possible
3) ACC reference level fine adjustment
4) Parameter for burst level fine adjustment
5) Threshold level at which chroma amplitude becomes valid is selected based upon color burst ratio.
   0.5
   0.25*
   0.125
   Off
   Off: The color killer function is turned off. If decoloration occurs while decoding a still picture, setting the threshold level to "off" will reduce the decoloration.
6) Color killer mode selection
   Auto color killer mode*
   Forced color killer
7) Parameter for fine adjustment of color subcarrier phase

In this block, chroma signals pass through a bandpass filter to cut out unnecessary band.
To maintain a constant chroma level, these signals then pass through an ACC compensating circuit and are UV demodulated. (The filter can be bypassed.)
If the demodulated result does not reach a constant level, color killer signals are generated to fix the ACC gain. This functions as an auto color killer control circuit.
The UV demodulated results pass through a low-pass filter and are output as chrominance signals.

4. Synchronization Block

This block processes the sync signals. Synchronous signals are generated for chip output and for internal use. Various signals are output from this block and the following operating modes can be selected.

1) Adjustment of SYNC threshold level (internal sync)
2) HSY control
   2-1) Fine adjustment of HSY signal (start side)
   2-2) Fine adjustment of HSY signal (stop side)
3) HSY signal enable selection
   High Level*
   Active
   Low Level
   The HSY signal provides the sync-tip-clamp processing for the A/D converter.
4) Fine adjustment of HSYNC_L signal
5) HVALID control
   5-1) Fine adjustment of HVALID signal (start side)
   5-2) Fine adjustment of HVALID signal (stop side)
6) VVALID control
   6-1) Fine adjustment of VVALID signal (start side)
   6-2) Fine adjustment of VVALID signal (stop side)
   Data signals are transferred at the rising edge of the HVALID signal.
7) FIFO and Field Memory mode selection
   FIFO-1 mode*: Sets and outputs a standard value for the number of pixels per 1H from the internal FIFO.
   This mode is also compatible (to a degree) with non-standard VTR signals.
   FIFO-2 mode: Sets and outputs a constant pixel number corresponding to the input H interval for the number of pixels per 1H from the internal FIFO.
   FM-1 mode: This mode outputs the decoded results according to the SYNC signal.
   Usage of external field memory is required to manage the number of pixels and to absorb jitter.
   Memory control signals are to be generated externally.
   FM-2 mode: This mode is compatible with considerably distorted non-standard VTR signals. Jitter is absorbed by using external field memory (2 Mb × 2) and the standard value is set as the pixel number.
   Field memory control signals are output simultaneously from M[7:4].
8) Field memory control signals
   If the FM-1 mode uses external field memory (2 Mb × 2) instead of the internal FIFO, field memory control signals are supplied from pins M[7:4].

5. Epilogue Block

The Epilogue Block outputs the UV signal from the Chrominance block and the Y signal from the Luminance block in a format based on a signal obtained from the control register setting. This block can select the following modes.

1) Output mode selection
   1-1) ITU-RBT.656 (SAV, EAV, blank processing)
   1-2) * 8-bit (YCbCr) output (2x pixel clock) synchronization with HSYNC_L, VSYNC_L
   1-3) 16-bit (8-bit Y/8-bit CbCr) (pixel clock) synchronization with HSYNC_L, VSYNC_L
   1-4) 24-bit RGB (8 bits each) synchronization with HSYNC_L, VSYNC_L
2) Enable Blue Back display when synchronization fails
   OFF
   ON*
3) Selection of YCbCr signal output format
   YCbCr 4 : 2 : 2*
   YCbCr 4 : 1 : 1
   The chrominance signal (U, V component) outputs Cb and Cr data to the C pin in an output format to be described later.
4) Selection of 8-bit chroma signal output format
   Offset binary*
   2's complement
5) Output pin enable selection
   High-impedance
   Output enable*
6) Multiplex signal (VBI data) detection level adjustment
   The levels to detect multiplexed signals sent during the vertical blanking period are configured to be variable. The binary values after input signals are A-to D converted are employed as the levels to detect multiplexed signals, and the levels are set in eight steps with respect to the SYNC tip level. (See page 26 and page 27)
7) Various mode detection
   NTSC/PAL detection
   Multiplex signal detection
   HSYNC synchronization detection
   Iunternal FIFO overflow detection
8) Output signal phase control
   Y and C phases can each be adjusted in the range of –2 to +1 pixels.

6. I²C Control Block

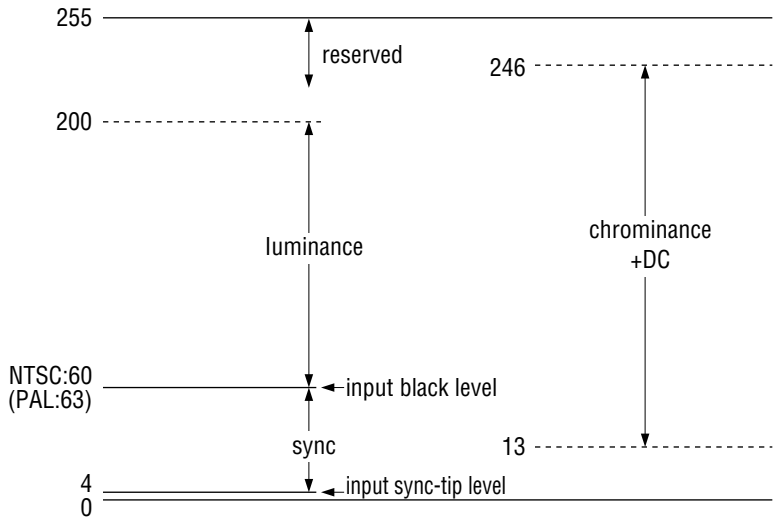
This serial interface block is based on the I²C standard of the Phillips Corporation.
This block only functions as a Slave-Receiver (write mode).

7. Test Control Block

This block is used to test the LSI chip. Normally this block is not used.

Input Signal Level

The figure below shows the ideal range of the input signal, considered as an 8-bit straight binary value.



NTSC/PAL: CVBS[7:0] input range

The above input conditions are ideal. Because analog signals are normally input at different levels, the exact settings described above are difficult to achieve. While maintaining the ratio of White Peak (100%)/SYNC = 100IRE/40IRE (NTSC), if the input signal is set within the A/D converter's voltage range, the Y digital output will be output with Black Level = 16 and White Peak (100%) = 235.

Output format

ITU-RBT.656 output, 8-bit (YCbCr) output, and 16-bit (8-bit Y/8-bit CbCr) output have the following formats.

The YCbCr 4:2:2 format and 4:1:1 format are shown below.
The output format can be changed by register settings.

Output	Pixel Byte Sequence					
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
C7 (MSB)	Cb7	Cr7	Cb7	Cr7	Cb7	Cr7
C6	Cb6	Cr6	Cb6	Cr6	Cb6	Cr6
C5	Cb5	Cr5	Cb5	Cr5	Cb5	Cr5
C4	Cb4	Cr4	Cb4	Cr4	Cb4	Cr4
C3	Cb3	Cr3	Cb3	Cr3	Cb3	Cr3
C2	Cb2	Cr2	Cb2	Cr2	Cb2	Cr2
C1	Cb1	Cr1	Cb1	Cr1	Cb1	Cr1
C0 (LSB)	Cb0	Cr0	Cb0	Cr0	Cb0	Cr0
Y point	0	1	2	3	4	5
C point	0		2		4	

YCbCr 4:2:2 format

Output	Pixel Byte Sequence							
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
C7 (MSB)	Cb7	Cb5	Cb3	Cb1	Cb7	Cb5	Cb3	Cb1
C6	Cb6	Cb4	Cb2	Cb0	Cb6	Cb4	Cb2	Cb0
C5	Cr7	Cr5	Cr3	Cr1	Cr7	Cr5	Cr3	Cr1
C4	Cr6	Cr4	Cr2	Cr0	Cr6	Cr4	Cr2	Cr0
C3	0	0	0	0	0	0	0	0
C2	0	0	0	0	0	0	0	0
C1	0	0	0	0	0	0	0	0
C0 (LSB)	0	0	0	0	0	0	0	0
Y point	0	1	2	3	4	5	6	7
C point	0				4			

YCbCr 4:1:1 format

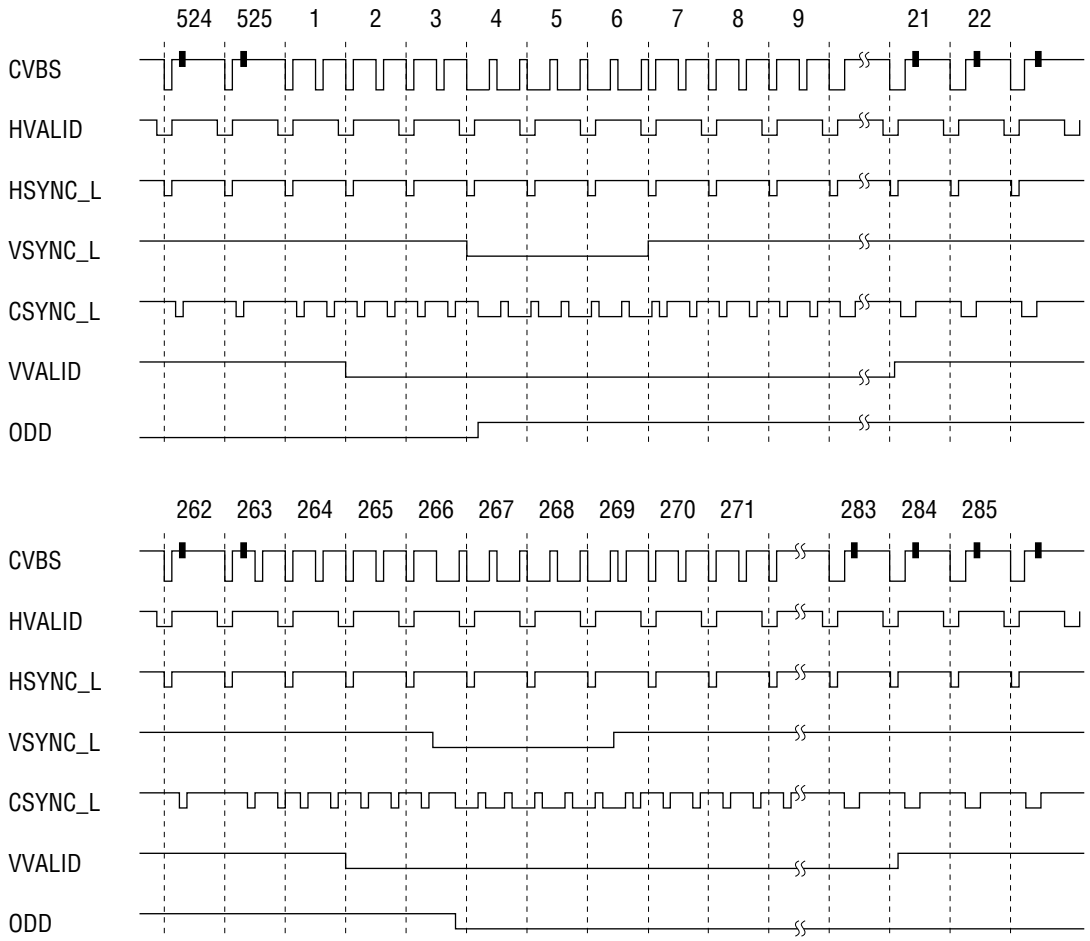
Relation between video mode and pixel number (default settings when standard signal is input)

Video Mode	Pixel Type	Pixel Rate (MHz)	Total Pixels	Active Pixels	Front-Porch	Hsyc Back-Porch	HBLK Total
NTSC	ITUR.601	13.5	858	720	16	122	138
	Square pixel	12.27	780	640	28	112	140
	4fsc	14.32818	910	768	8	134	142
PAL	ITUR.601	13.5	864	720	12	132	144
	Square pixel	14.75	944	768	34	142	176

TIMING DESCRIPTION

Vertical Synchronizing Signal

The vertical synchronizing signal timing is as follows.

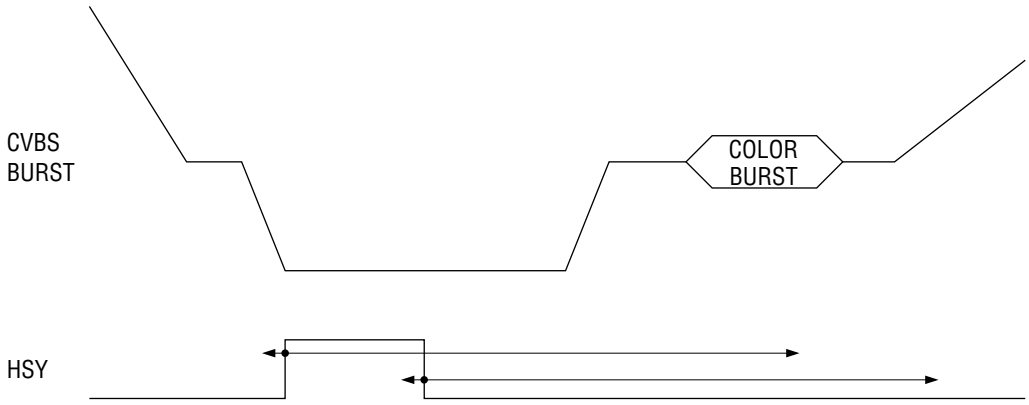


Vertical Synchronizing Signal (60 Hz)

Vertical Synchronizing Signal (50 Hz)

A/D Converter Support Signal

The waveform of the HSY signal, shown below, provides clamp timing to the A/D converter when HSY clamp (digital clamp) is selected. The start and end edges of the clamp pulse have a variable range from the sync chip to the pedestal position.

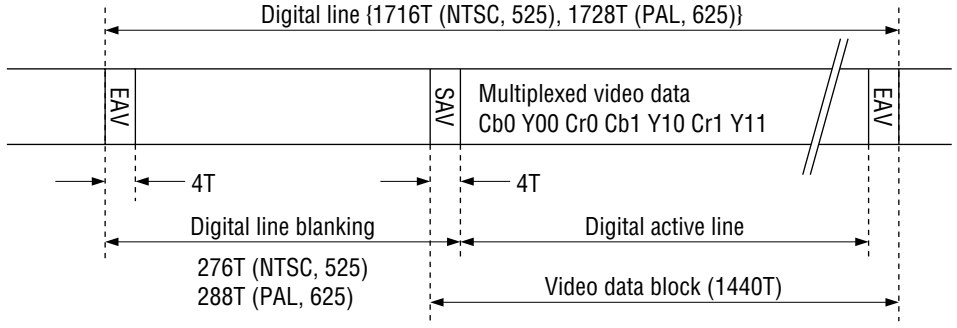


A/D Converter Support Signal

Output Timing

• ITU-R.656 output

T : clock periods 37 ns normal (1/27 MHz)
SAV : start of active video timing reference code
EAV : end of active video timing reference code



ITU-R BT.656 Output (Data in one line in which video data presents)

During the blanking interval, data is output with the Y value.

Note: Digital line 1716T (NTSC, 525) and 1728T (PAL, 625) are not maintained at the next line. Digital active line 1440T of the line immediately after VVALID falls and the 10th or 11th line after VSYNC_L rises will fluctuate due to pixel compensation. Especially when a non-standard signal is input, the line immediately after VVALID falls will fluctuate largely due to instability of the input signal. Due to phenomena such as an increase in the number of lines for a standard signal and a decrease in the number of lines for a non-standard signal, it may not be possible to guarantee correct EAV and SAV functionality.

Contents of SAV and EAV

Both SAV and EAV consist of 4 words. Their configuration is shown below.

Word	Bit No.								
	7 (MSB)	6	5	4	3	2	1	0 (LSB)	F = 0: during field 1
First	1	1	1	1	1	1	1	1	1: during field 2
Second	0	0	0	0	0	0	0	0	V = 0: elsewhere
Third	0	0	0	0	0	0	0	0	1: during field blanking
Fourth	1	F	V	H	P3	P2	P1	P0	H = 0: SAV H = 1: EAV

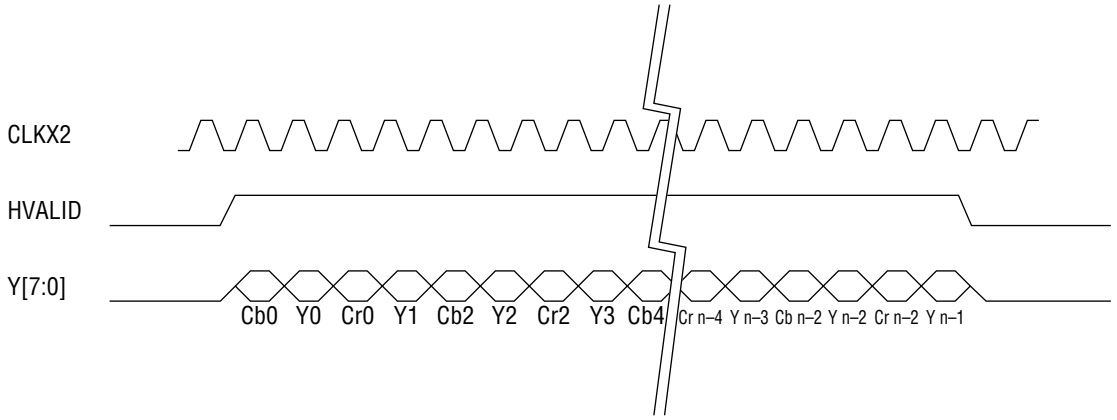
P3, P2, P1, P0: Protection bit

The 4th word of SAV and EAV

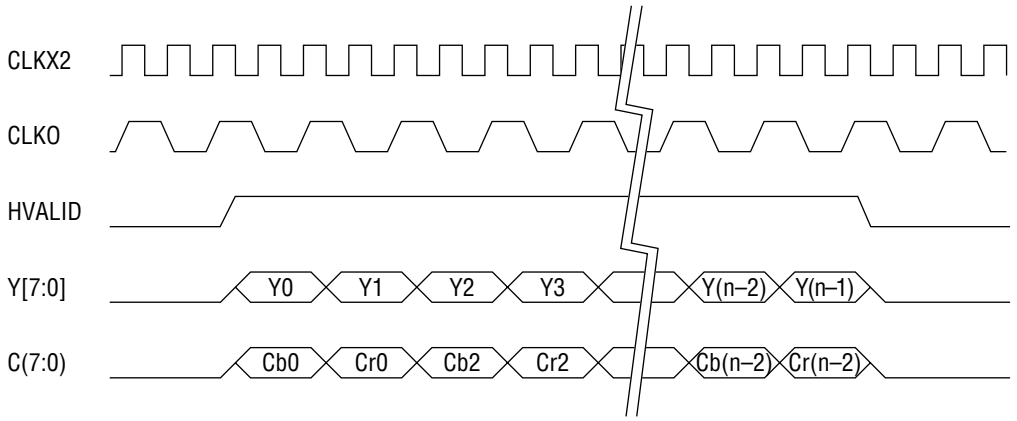
The relationship between the F, V, H and Protection bits in the 4th word of SAV and EAV is shown below.

Bit No.	7 (MSB)	6	5	4	3	2	1	0
Function	Fixed 1	F	V	H	P3	P2	P1	P0
0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1
2	1	0	1	0	1	0	1	1
3	1	0	1	1	0	1	1	0
4	1	1	0	0	0	1	1	1
5	1	1	0	1	1	0	1	0
6	1	1	1	0	1	1	0	0
7	1	1	1	1	0	0	0	1

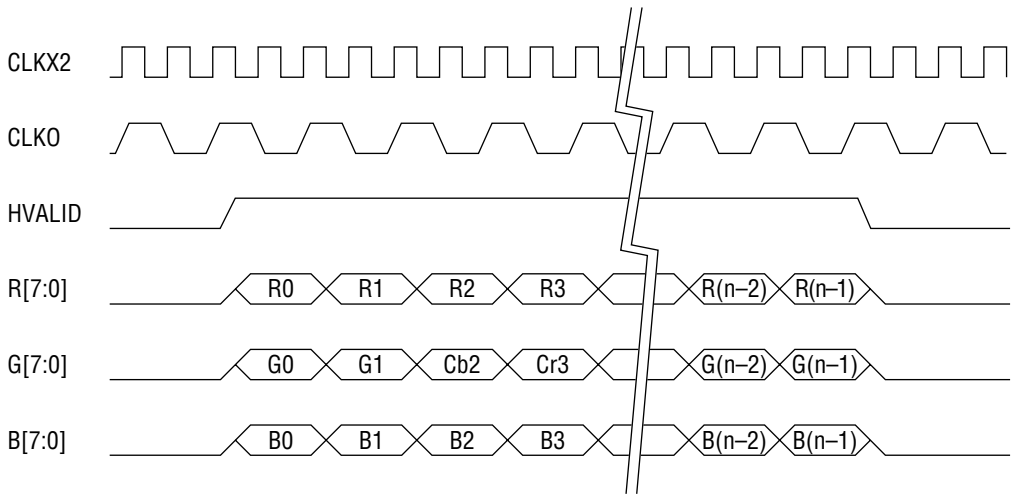
Usually, V = 1 during blanking, however when VBI data is detected and V = 0 is the desired output, set the MRC[3] SAV, EAV V-status of Mode Register C (MRC) to "1".



8-bit (YCbCr: 2x clock) Output



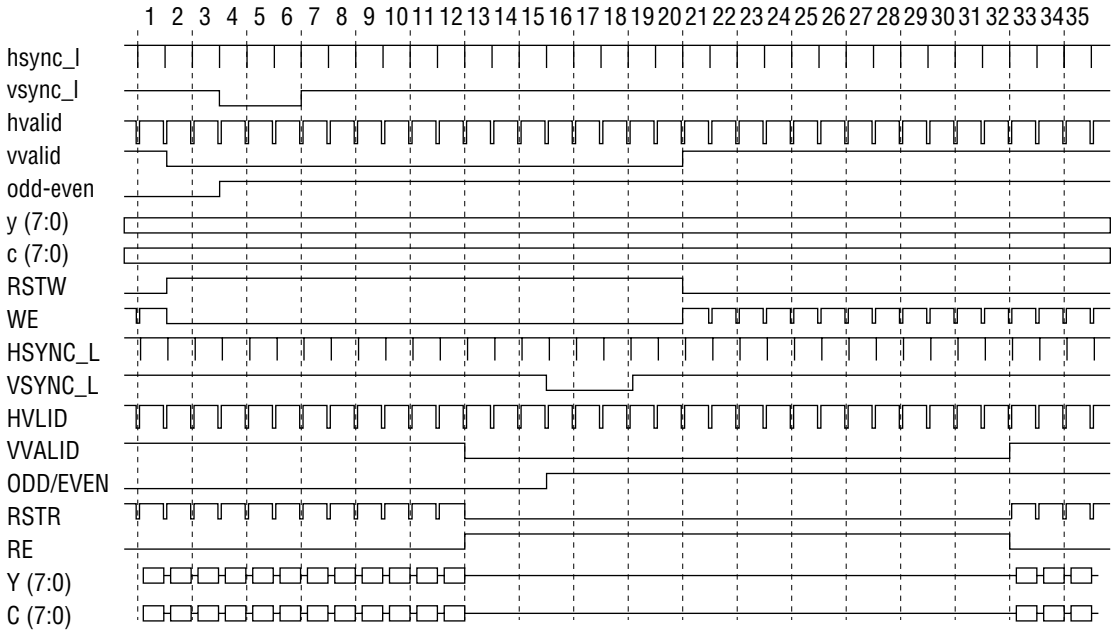
16-bit (Y: 8-bit, CbCr: 8-bit) Output



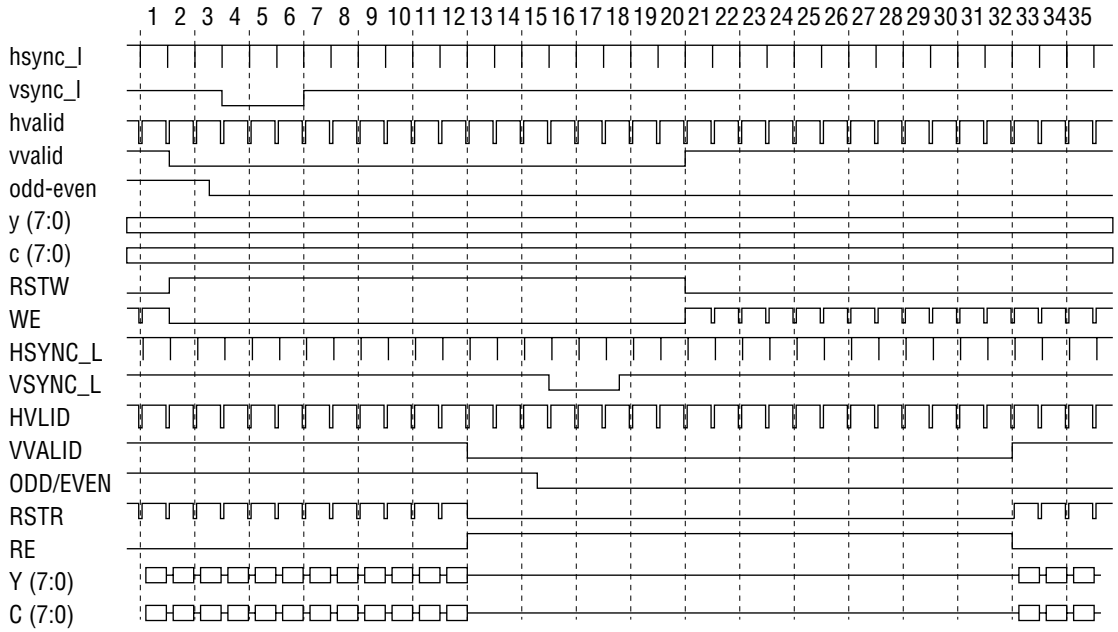
24-bit (R: 8-bit, G: 8-bit, B: 8-bit) Output

• Timing when using external field memory
Field memory timing in the FM-2 mode, using control signals from the decoder
Field memory: MSM518222, 2 units are used (Y and C)
Four memory control signals are supplied from the decoder, M[4]: RSTW, M[5]: RSTR, M[6]: WE:, and M[7]: RE.

NTSC Signal (13.5 MHz)

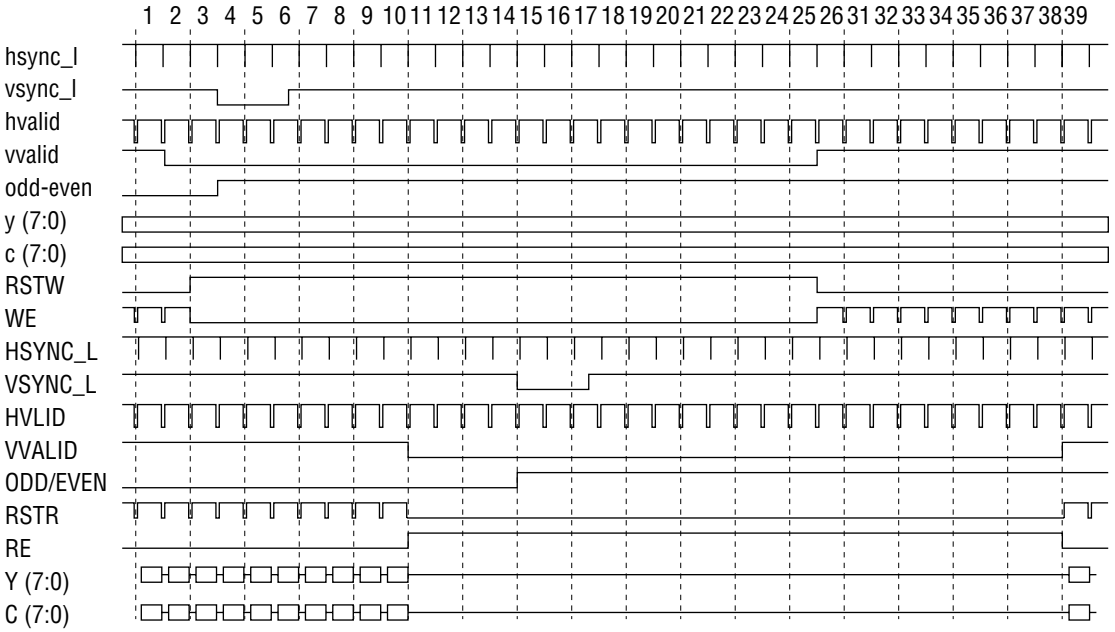


NTSC: ODD Field

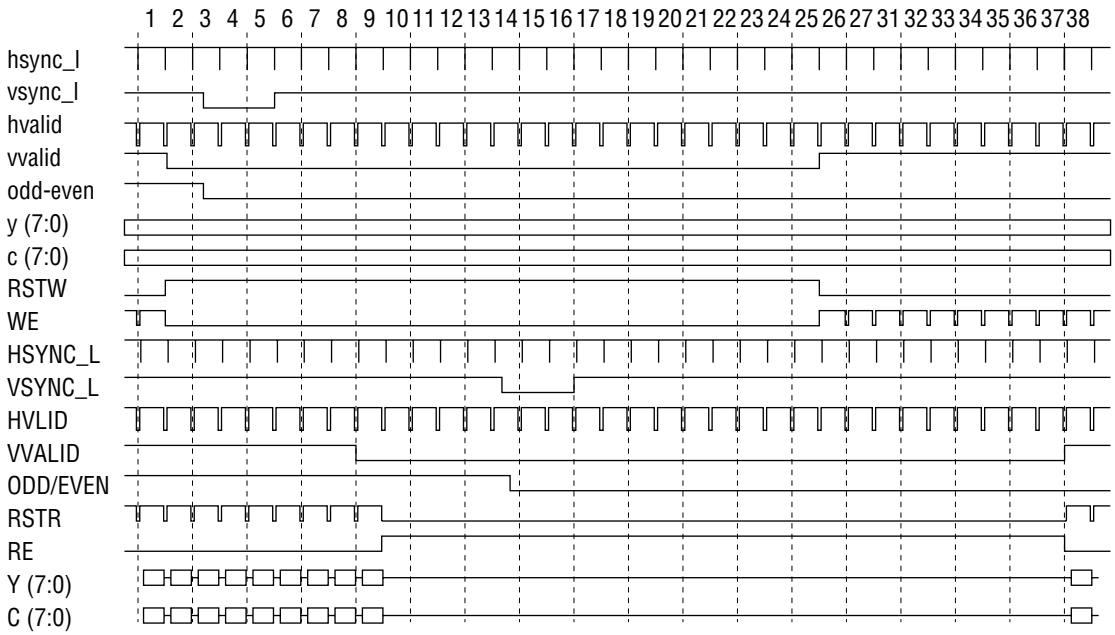


NTSC: EVEN Field

PAL Signal (13.5 MHz)



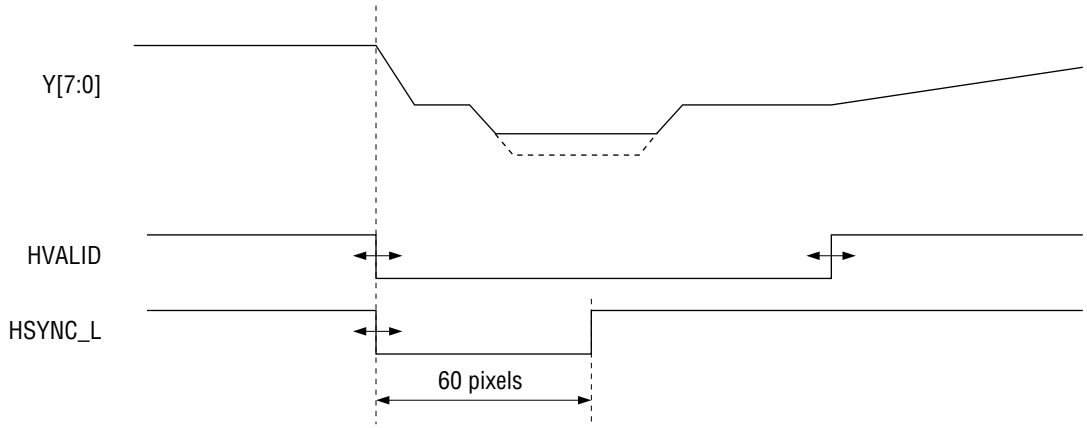
PAL: ODD Field



PAL: EVEN Field

Horizontal Synchronization Signal

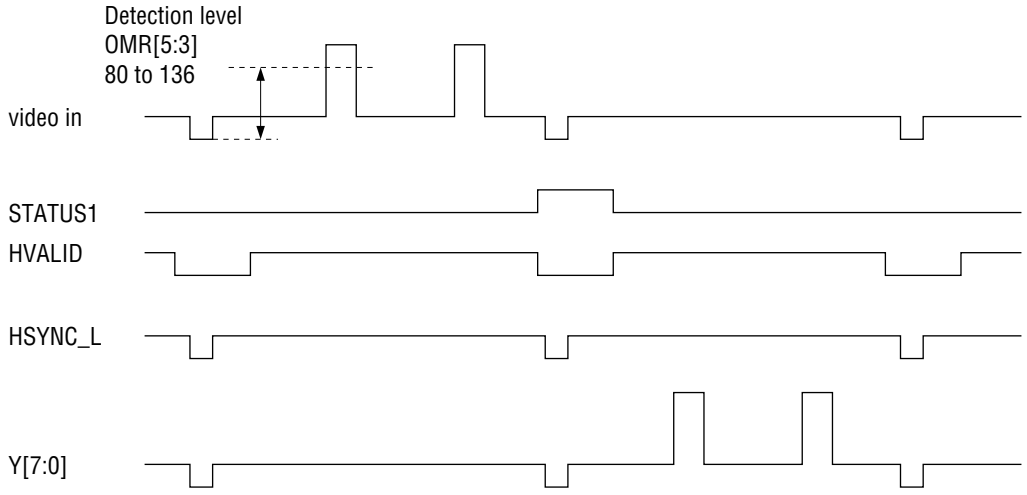
The horizontal synchronization signal timing is shown below.



Horizontal Timing

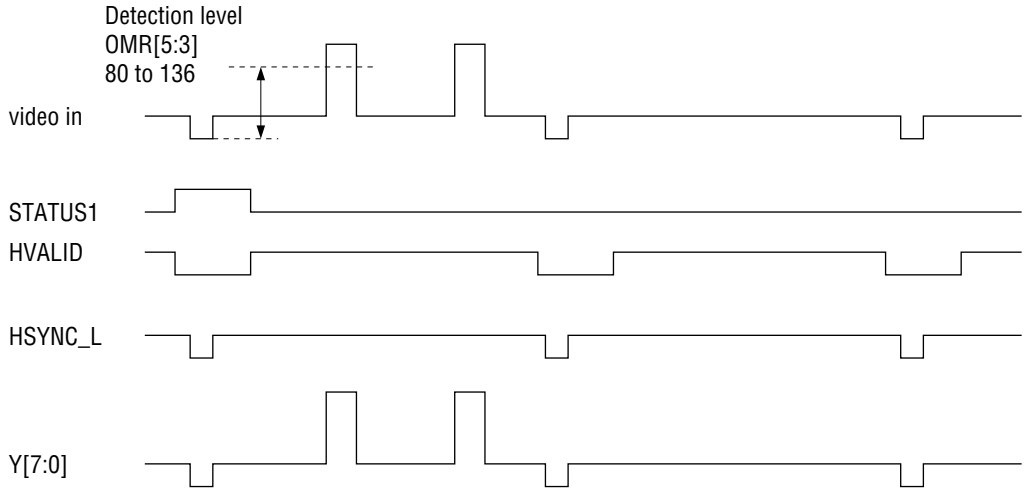
VBI Data Detection (when a Composite signal is input): STATUS1 Timing

VBI data detection results are output from the STATUS1 pin.



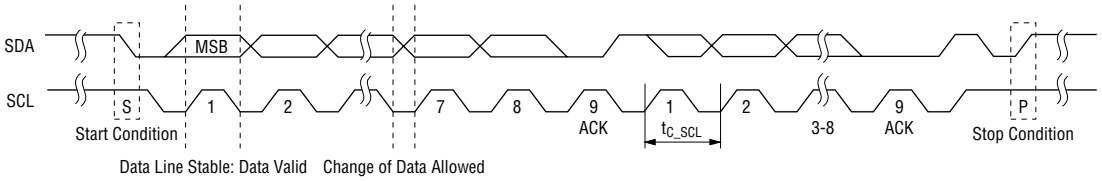
VBI Data Detection (when an S-Video signal is input): STATUS1 Timing

VBI data detection results are output from the STATUS1 pin.



I²C-bus Interface Input and Output Timing

Basic input and output timing of the I²C-bus interface is shown below.



I²C-bus Basic Input/Output Timing

I²C BUS FORMAT

The I²C-bus interface input format is shown below.

S	Slave Address	A	Subaddress	A	Data 0	A	·····	Data n	A	P

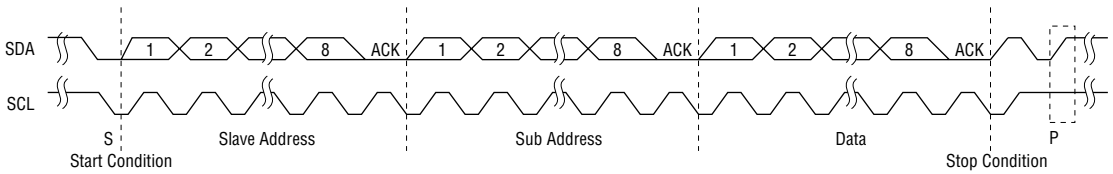
Symbol	Description
S	Start condition
Slave Address	Slave address 1000001X, 8th bit is write signal ["0"] or read signal ["1"]
A	Acknowledge. Generated by slave
Subaddress	Subaddress byte
Data n	Data to write to address designated by subaddress.
P	Stop condition

As mentioned above, the write operation can be executed from subaddress to subaddress continuously. When the write operation is executed at subaddresses discontinuously, the Acknowledge and Stop condition formats are input repeatedly after Data 0.

If one of the following matters occurs, the decoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The write attribute of a register does not match "X" (read ["1"]/write ["0"] control bit).

The input timing is shown below.



OPERATING MODE SETTING

There are two types of video mode settings.
1. External pin mode: direct setting from dedicated pins
2. Register setting mode: specification by internal register settings

These modes can be switched by the mode register MRA[0].
The reset state (default) is the external pin mode.

The following registers can be set in the external pin mode.

MRA[3:1]	Input signal mode	*000: NTSC ITU-RBT.601	13.5 MHz
		001: NTSC Square Pixel	12.27 MHz
		010: NTSC 4fsc	14.31818 MHz
		100: PAL ITU-RBT.601	13.5 MHz
		101: PAL Square Pixel	14.75 MHz
MRA[7:6]	Output mode	00: ITU-R BT.656 (SAV, EAV, blank processing)	
		*01: 8 bit (Y CbCr) HSYNC_L and VSYNC_L used for synchronization	
		10: ITU-R BT.601 16 bit (8 bit Y, 8 bit CbCr)	
		11: RGB (8 bit R, 8 bit G, 8 bit B)	

Note: NTSC 4fsc cannot be set externally.

Pin Setting Example

NTSC, 27 MHz (ITU-RBT.601), Composite input, 8-bit (YCbCr) Output

Pin name	Condition	Notes
MODE[3]	= low	0 : ITU-RBT.656 01 : 8-bit (YCbCr)
MODE[2]	= high	10 : 16-bit (Y + CbCr) 11 : RGB
MODE[1]	= low	0 : NTSC 1 : PAL
MODE[0]	= low	0 : ITU-RBT.601 1 : Square Pixel
CLKSEL	= low	0 : twice the pixel frequency 1 : pixel frequency
PLLSEL	= low	Normally set to a low level
INS[2:0]	= low	
GAINS[2:0]	= low	
TEST[2:0]	= low	
SCAN	= low	
M[2]	=	: low = 1000001, : high = 1000011
M[1]	= low	Normally set to a low level
M[0]	= low	
SLEEP	=	0 : normal operation 1 : sleep operation

INTERNAL REGISTERS

Register List

Register Function	Write /Read	Sub-address	Data byte							
			D7	D6	D5	D4	D3	D2	D1	D0
Mode Register A (MRA)	Write	0	MRA7	MRA6	MRA5	MRA4	MRA3	MRA2	MRA1	MRA0
Mode Register B (MRB)	Write	1	MRB7	MRB6	MRB5	MRB4	MRB3	MRB2	MRB1	MRB0
Mode Register C (MRC)	Write	2	MRC7	MRC6	MRC5	MRC4	MRC3	MRC2	MRC1	MRC0
Horizontal Sync Trimmer (HSYT)	Write	3	HSYT7	HSYT6	HSYT5	HSYT4	HSYT3	HSYT2	HSYT1	HSYT0
Sync Threshold level adjust (STHR)	Write	4	STHR7	STHR6	STHR5	STHR4	STHR3	STHR2	STHR1	STHR0
Horizontal Sync Delay (HSDL)	Write	5	HSDL7	HSDL6	HSDL5	HSDL4	HSDL3	HSDL2	HSDL1	HSDL0
Horizontal Valid Trimmer (HVALT)	Write	6	HVALID7	HVALID6	HVALID5	HVALID4	HVALID3	HVALID2	HVALID1	HVALID0
Vertical Valid Trimmer (VVALT)	Write	7	VVALID7	VVALID6	VVALID5	VVALID4	VVALID3	VVALID2	VVALID1	VVALID0
Luminance Control (LUMC)	Write	8	LUMC7	LUMC6	LUMC5	LUMC4	LUMC3	LUMC2	LUMC1	LUMC0
AGC/Pedestal Loop filter Control (AGCLF)	Write	9	AGCLF7	AGCLF6	AGCLF5	AGCLF4	AGCLF3	AGCLF2	AGCLF1	AGCLF0
Sync separation level (SSEPL)	Write	A	SSEPL7	SSEPL6	SSEPL5	SSEPL4	SSEPL3	SSEPL2	SSEPL1	SSEPL0
Chrominance Control (CHRC)	Write	B	CHRC7	CHRC6	CHRC5	CHRC4	CHRC3	CHRC2	CHRC1	CHRC0
ACC Loop filter Control (ACCLF)	Write	C	ACCLF7	ACCLF6	ACCLF5	ACCLF4	ACCLF3	ACCLF2	ACCLF1	ACCLF0
Hue Control (HUE)	Write	D	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Output phase Control for Data Y (OPCY)	Write	E	OPCY7	OPCY6	OPCY5	OPCY4	OPCY3	OPCY2	OPCY1	OPCY0
Output phase Control for Data C (OPCC)	Write	F	OPCC7	OPCC6	OPCC5	OPCC4	OPCC3	OPCC2	OPCC1	OPCC0
Optional Mode Register (OMR)	Write	10	OMR7	OMR6	OMR5	OMR4	OMR3	OMR2	OMR1	OMR0
ADC register (ADC1)	Write	11	ADC17	ADC16	ADC15	ADC14	ADC13	ADC12	ADC11	ADC10
ADC register (ADC2)	Write	12	ADC27	ADC26	ADC25	ADC24	ADC23	ADC22	ADC21	ADC20
ADC register (ADC3)	Write	13	ADC37	ADC36	ADC35	ADC34	ADC33	ADC32	ADC31	ADC30
0 level detect register (ZLD)	Write	14	ZLD7	ZLD6	ZLD5	ZLD4	ZLD3	ZLD2	ZLD1	ZLD0
Stataus register (STATUS)	Read	20	STATUS7	STATUS6	STATUS5	STATUS4	STATUS3	STATUS2	STATUS1	STATUS0

Register Parameters

Registers controlled from the I²C-bus are listed below.
An asterisk (*) indicates that the register setting value is the default value.

Mode Register A (MRA) Write only <address: $00>

MRA[7:6]	Video output mode	00: ITU-R BT.656 (SAV, EAV, blank processing)	
		*01: Y,C 8 bits (SAV, EAV, without blank processing)	
		10: Y,C 16 bits	
		11: RGB 24 bits	
MRA[5]	Chroma format	*0: Offset binary	
		1: 2's Complement	
MRA[4]	Video input model	*0: Composite video input	
		1: S-video input	
MRA[3:1]	Video Input mode2	*000: NTSC ITU-R BT.601	13.5 MHz
		001: NTSC Square Pixel	12.27 MHz
		010: NTSC 4fsc	14.31818 MHz
		100: PAL ITU-R BT.601	13.5 MHz
		101: PAL Square Pixel	14.75 MHz
MRA[0]	Disable MODE[3:0] pin	*0: External pin mode	
		1: Register mode	

Mode Register B (MRB) Write only <address: $01>

MRB[7:6]	Synchronization mode	*00: FIFO-1 (use internal memory)
		01: FIFO-2 (use internal memory)
		10: FM-1 (use external memory, external control)
		11: FM-2 (use external memory, control signals supplied from M[7:4])
MRB[5]	Color killer mode	*0: Auto color killer (Chrominance signal level is set to "0" if the color burst level is below the specified value.)
		*1: Forced color killer (Chrominance signal level is forced to "0".)
MRB[4]	Blue Back	0: OFF (Video signal is demodulated and output regardless of synchronization detection.)
		*1: AUTO (Blue Back is output when synchronization is not detected.)
MRB[3:2]	Clamp mode	*00: Analog Clamp (HSY = 1)
		01: Analog, HSY hybrid clamp
		10: HSY clamp
		11: HSY = 0
MRB[1:0]	Y/C separation mode	*00: Adaptive comb filter (Correlation of 3 lines is monitored and operating mode is selected.)
		01: Non-adaptive comb filter (Operating mode is always fixed.)
		10: Use trap filter. (Comb filter is not used.)
		11: Undefined

Note:	Adaptive comb filter	2/3-line comb filter for NTSC Comb filter/trap filter for PAL
	Non-adaptive comb filter	3-line comb filter for NTSC 2-line cosine comb filter for PAL

Mode Register C (MRC) Write only <address: $02>

MRC[7]	NTSC/PAL Auto select	0: Fix *1: Auto
MRC[6]	Sub Pixel Alignment	*0: Use pixel position compensating circuit. 1: Do not use pixel position compensating circuit.
MRC[5]	Pixel Sampling Rate	*0: (4:2:2) 1: (4:1:1)
MRC[4]	Data-pass control	*0: Use DECIMATOR at 2x sampling 1: Do not use DECIMATOR

Note: This register is valid when a 2x clock (27 MHz) is input.

MRC[3]	SAV, EAV V-status	*0: During blanking, V = 1 1: During blanking, while VBI data is not detected, V = 1
MRC[2]	RGB output level	*0: 0 to 255 1: 16 to 235
MRC[1:0]	Undefined	Set to 0

Horizontal Sync Trimmer (HSYT) Write only <address: $03>

HSYT[7:4]	HSY start trimmer (× 8 pixels)	$C to $B (*$0): –4 to +11 (–32 to +88 pixels)
HSYT[3:0]	HSY stop trimmer (× 8 pixels)	$C to $B (*$0): –4 to +11 (–32 to +88 pixels)

Sync. Threshold level adjust (STHR) Write only <address: $04>

STHR[7:0]	Sync. depth	$00 to $FF (*$1E): 0 to 255

Horizontal Sync Delay (HSDL) Write only <address: $05>

HSDL[7:0]	HSYNC_L delay trimmer (× 1 pixel)	$80 to $7F (*$00): –128 to +127 (–128 to +127 pixels)

Note: In the internal sync separation (PLLSEL: Low) mode, the HSYNC_L sync signal output position is adjusted.
In the external sync separation (PLLSEL: High) mode, the phase shift of the H-Sync input and video signal input is adjusted.

Horizontal Valid Trimmer (HVALT) Write only <address: $06>

HVALT[7:4]	HVALID start trimmer (× 2 pixels)	$8 to $7 (*$0): –8 to +7 (–16 to +14 pixels)
HVALT[3:0]	HVALID stop trimmer (× 2 pixels)	$8 to $7 (*$0): –8 to +7 (–16 to +14 pixels)

Vertical Valid Trimmer (VVALT) Write only <address: $07>

VVALT[7:4]	VVALID start trimmer (× 1 line)	$8 to $7 (*$0): –8 to +7
VVALT[3:0]	VVALID stop trimmer (× 1 line)	$8 to $7 (*$0): –8 to +7

Luminance Control (LUMC) Write only <address: $08>

LUMC[7]	Output level limiter	*0: OFF 1: ON
Note: Control range while limiter is ON: 16...235		
LUMC[6]	Use of Pre-filter	*0: Do not use prefilter 1: Use prefilter
LUMC[5:4]	Aperture bandpass select	*00: range0 (middle) 01: range1 10: range2 11: range3 (high)
LUMC[3:2]	Coring range select	*00: coring off 01: +/–4LSB 10: +/–5LSB 11: +/–7LSB
LUMC[1:0]	Aperture filter weighting factor	*00: 0.00 01: 0.25 10: 0.75 11: 1.50

AGC/Pedestral Loop filter control (AGCLF)
Write only <address: $09>

AGCLF[7:6]	AGC loop filter time constant	00: slow *01: medium 10: fast 11: MGC mode
AGCLF[5:0]	AGC reference level	$20 to $1F (*$00): –32 to +31

Sync separation level (SSEPL) Write only <address: $0A>

SSEPL[7]	Pedestal Clamp on/off	*0: Do not use pedestal clamp 1: Use pedestal clamp (AGC stops operating)
SSEPL[6:0]	Sync. separation level	$40 to $3F (*$00): –64 to +63

Chrominance Control (CHRC) Write only <address: $0B>

CHRC[7:4]	Undefined	Set 0
CHRC[3]	C-Output level limiter	*0: OFF 1: ON
Note: Control range while limiter is ON: 16...224		

CHRC[2]	Chroma bandpass filter	0: OFF *1: ON
CHRC[1:0]	Color kill threshold factor	00: 0.500 color burst level *01: 0.250 color burst level 10: 0.125 color burst level 11: Color killer off

ACC Loop filter control (ACCLF)

Write only <address: $0C>

ACCLF[7]	Undefined	Set 0
ACCLF[6:5]	ACC loop filter time constant	00: slow *01: medium 10: fast 11: MCC mode
ACCLF[4:0]	ACC reference level	$10 to $0F (*$00): –16 to +15

Hue control (HUE) Write only <address: $0D>

HUE[7:0]	Hue control	$80 to $7F (*$00): –180 to +178.6 degrees

Output phase control for data Y (OPCY)

Write only <address: $0E>

OPCY[7:2]	Undefined	Set 0
OPCY[1:0]	Output phase control for data Y	*00: normal 01: forward l clock 10: backward 2 clock 11: backward l clock

Output phase control for data C (OPCC)

Write only <address: $0F>

OPCC[7:2]	Undefined	Set 0
OPCC[1:0]	Output phase control for data C	*00: normal 01: forward l clock 10: backward 2 clock 11: backward l clock

Optional Mode Register (OMR)

Write only <address: $10>

OMR[7]	HSY output timing select	*0: Use A/D clamp position adjust circuit 1: Do not use A/D clamp position adjust circuit

OMR[6]	VSYNC output timing select	*0: VSYNC_L is synchronized to HSYNC_L and then output 1: VSYNC_L is output when a VSYNC input signal is detected.
OMR[5:3]	Multiplex signal detection level (VBID etc.)	000: 80 001: 88 *010: 96 011: 104 100: 112 101: 120 110: 128 111: 136
OMR[2]	Hi-Z Output in SLEE MODE	*0: Active 1: Hi-Z
OMR[1]	Status2 output mode	*0: NTSC/PAL identification 1: HLOCK sync detection
OMR[0]	Status3 output mode	*0: TV/VCR identification 1: CSYNC

ADC register 1 (ADC1) Write only <address: $11>

ADC1[7]	Video amp select	*0: Use 1: Do not use
ADC1[6]	Comparator select	*0: Use 1: Do not use
ADC1[5:4]	Clamp current select	*00: 1.0 01: 1.5 10: Undifined 11: 2.0
ADC1[2:0]	ADC input select	*000: ADI-VIN1 (composite) 001: ADI-VIN2 (composite) 010: ADI-VIN3 (composite) 011: ADI-VIN4 (composite) 100: ADI-VIN5 (composite) 101: ADI-VIN1 (Y), AD2-VIN5 (C) 110: ADI-VIN2 (Y), AD2-VIN6 (C) 111: Prohibited setting (ADC enters sleep state)

ADC register 2 (ADC2) Write only <address: $12>

ADC2[7]	ADC gain control mode select	0: manual *1: auto
ADC2[6:4]	ADC gain manual select	000: 1.00 *001: 1.35 010: 1.75 011: 2.30 100: 3.00

101: 3.80
110: 5.00
111: 2.05

ADC2[3] ADC initialize condition gain select
0: not initialize
*1: initialize

ADC2[1:0] ADC gain control and stage select
00: 2nd change end
01: 3rd change end
*10: 3rd change loop

ADC register 3 (ADC3) Write only <address: $13>

ADC3[7] Undefined Set 0

ADC3[6:4] ADC gain control margin level select
000: 10 mV
001: 20 mV
*010: 40 mV
011: 80 mV
100: 160 mV

ADC3[2:0] ADC gain control line select
000: 1 line
001: 2 lines
*010: 4 lines
011: 8 lines
100: 16 lines

0 level detect register (ZLD) Write only <address: $14>

ZLD[7:3] Undefined Set 0

ZLD[2:0] 0 level detect width (× 8 pixel)
000: Undefined
001: 8 pixels
*010: 16 pixels
011: 24 pixels
100: 32 pixels
101: 40 pixels
110: 48 pixels
111: 56 pixels

Status register (STATUS) Read only <address: $20>

STATUS[7:5]	Undefined	
STATUS[4]	VBI interval multiplex signal detection	0: Non-detection, 1: Detection
STATUS[3]	HLOCK sync detection	0: Non-detection, 1: Detection
STATUS[2]	NTSC/PAL identification	0: NTSC, 1: PAL
STATUS[1]	TV1/TV2 identification Mode Register B (bit 6)	0: TV1, 1: TV2
STATUS[0]	FTFO overflow detection	0: Non-detection, 1: Detection

Relationship between Register Setting Value and Adjusted Value

Horizontal Sync Trimmer

Position adjustment of sync chip clamp timing signal

HSYT [7:4] :Adjusting the starting position

Register Setting Value (0x)	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
Adjusted Value (Pixel)	–32	–24	–16	–8	0	+8	+16	+24	+32	+40	+48	+56	+64	+72	+80	+88

HSYT [3:0] :Adjusting the end position

Register Setting Value (0x)	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
Adjusted Value (Pixel)	–32	–24	–16	–8	0	+8	+16	+24	+32	+40	+48	+56	+64	+72	+80	+88

Horizontal Sync Delay

Adjustment of the starting position of horizontal sync signal

HSDL [7:0]

		MSB[7 : 4]															
		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
LSB [3 : 0]	0	–128	–112	–96	–80	–64	–48	–32	–16	0	+16	+32	+48	+64	+80	+96	+112
	1	–127	–111	–95	–79	–63	–47	–31	–15	+1	+17	+33	+49	+65	+81	+97	+113
	2	–126	–110	–94	–78	–62	–46	–30	–14	+2	+18	+34	+50	+66	+82	+98	+114
	3	–125	–109	–93	–77	–61	–45	–29	–13	+3	+19	+35	+51	+67	+83	+99	+115
	4	–124	–108	–92	–76	–60	–44	–28	–12	+4	+20	+36	+52	+68	+84	+100	+116
	5	–123	–107	–91	–75	–59	–43	–27	–11	+5	+21	+37	+53	+69	+85	+101	+117
	6	–122	–106	–90	–74	–58	–42	–26	–10	+6	+22	+38	+54	+70	+86	+102	+118
	7	–121	–105	–89	–73	–57	–41	–25	–9	+7	+23	+39	+55	+71	+87	+103	+119
	8	–120	–104	–88	–72	–56	–40	–24	–8	+8	+24	+40	+56	+72	+88	+104	+120
	9	–119	–103	–87	–71	–55	–39	–23	–7	+9	+25	+41	+57	+73	+89	+105	+121
	A	–118	–102	–86	–70	–54	–38	–22	–6	+10	+26	+42	+58	+74	+90	+106	+122
	B	–117	–101	–85	–69	–53	–37	–21	–5	+11	+27	+43	+59	+75	+91	+107	+123
	C	–116	–100	–84	–68	–52	–36	–20	–4	+12	+28	+44	+60	+76	+92	+108	+124
	D	–115	–99	–83	–67	–51	–35	–19	–3	+13	+29	+45	+61	+77	+93	+109	+125
	E	–114	–98	–82	–66	–50	–34	–18	–2	+14	+30	+46	+62	+78	+94	+110	+126
	F	–113	–97	–81	–65	–49	–33	–17	–1	+15	+31	+47	+63	+79	+95	+111	+127

Horizontal Valid Trimmer

Position adjustment of horizontal valid pixel timing signal

HVALT [7:4] :Adjusting the starting position

Register Setting Value (0x)	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
Adjusted Value (Pixel)	–16	–14	–12	–10	–8	–6	–2	–1	0	+2	+4	+6	+8	+10	+12	+14

HVALT [3:0] :Adjusting the end position

Register Setting Value (0x)	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
Adjusted Value (Pixel)	–16	–14	–12	–10	–8	–6	–4	–2	0	+2	+4	+6	+8	+10	+12	+14

Vertical Valid Trimmer

Position adjustment of vertical valid line timing signal

VVALT [7:4] :Adjusting the starting position

Register Setting Value (0x)	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
Adjusted Value (Line)	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7

VVALT [3:0] :Adjusting the end position

Register Setting Value (0x)	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
Adjusted Value (Line)	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7

AGC Loop filter control

AGCLF [5:0] :Adjusting sync level

Register Setting Value (0x)		MSB [5 : 4]			
		2	3	0	1
LSB [3 : 0]	0	–32	–16	0	+16
	1	–31	–15	+1	+17
	2	–30	–14	+2	+18
	3	–29	–13	+3	+19
	4	–28	–12	+4	+20
	5	–27	–11	+5	+21
	6	–26	–10	+6	+22
	7	–25	–9	+7	+23
	8	–24	–8	+8	+24
	9	–23	–7	+9	+25
	A	–22	–6	+10	+26
	B	–21	–5	+11	+27
	C	–20	–4	+12	+28
	D	–19	–3	+13	+29
	E	–18	–2	+14	+30
	F	–17	–1	+15	+31

Sync separation level

SSEPL [6:0] :Adjusting the blanking level

Register Setting Value (Ox)		MSB [6 : 4]							
		4	5	6	7	0	1	2	3
	0	–64	–48	–32	–16	0	+16	+32	+48
	1	–63	–47	–31	–15	+1	+17	+33	+49
	2	–62	–46	–30	–14	+2	+18	+34	+50
	3	–61	–45	–29	–13	+3	+19	+35	+51
	4	–60	–44	–28	–12	+4	+20	+36	+52
	5	–59	–43	–27	–11	+5	+21	+37	+53
	6	–58	–42	–26	–10	+6	+22	+38	+54
LSB	7	–57	–41	–25	–9	+7	+23	+39	+55
[3 : 0]	8	–56	–40	–24	–8	+8	+24	+40	+56
	9	–55	–39	–23	–7	+9	+25	+41	+57
	A	–54	–38	–22	–6	+10	+26	+42	+58
	B	–53	–37	–21	–5	+11	+27	+43	+59
	C	–52	–36	–20	–4	+12	+28	+44	+60
	D	–51	–35	–19	–3	+13	+29	+45	+61
	E	–50	–34	–18	–2	+14	+30	+46	+62
	F	–49	–33	–17	–1	+15	+31	+47	+63

ACC Loop filter control

ACCLF [4:0] :Adjusting the color burst level

Register Setting Value (Ox)		MSB [4]	
		1	0
	0	–16	0
	1	–15	+1
	2	–14	+2
	3	–13	+3
	4	–12	+4
	5	–11	+5
	6	–10	+6
LSB	7	–9	+7
[3 : 0]	8	–8	+8
	9	–7	+9
	A	–6	+10
	B	–5	+11
	C	–4	+12
	D	–3	+13
	E	–2	+14
	F	–1	+15

Hue control

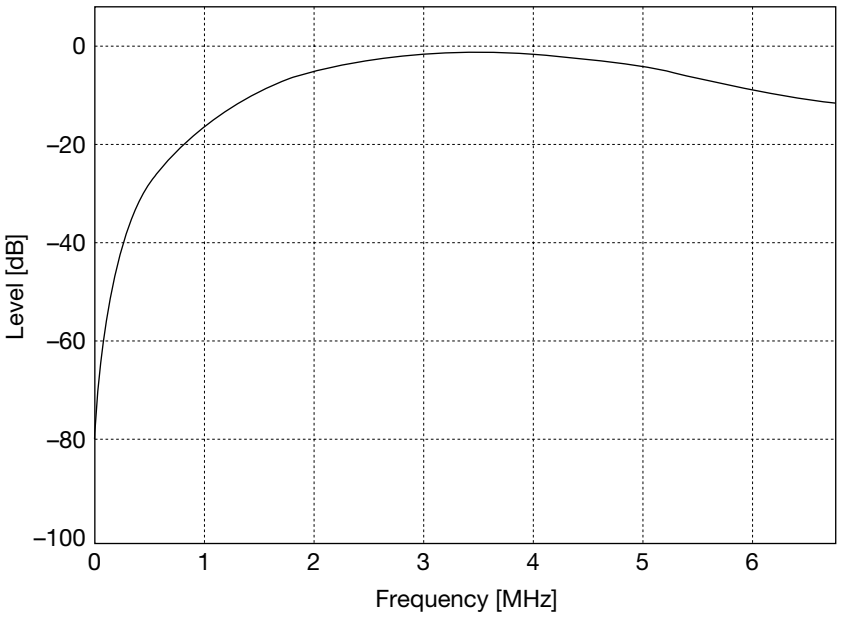
Adjustment of color subcarrier phase

HUE [7:0]

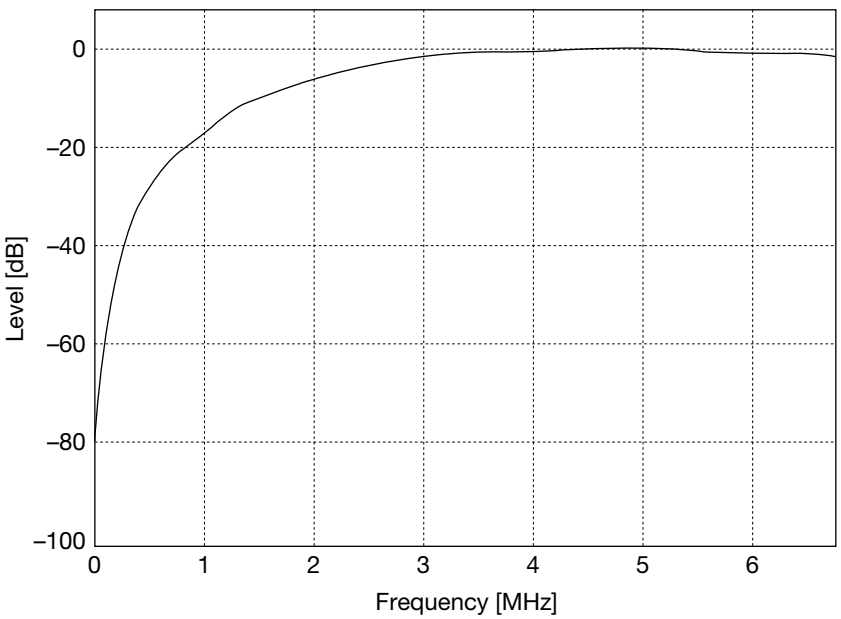
Register Setting Value (Ox)		MSB [7 : 4]															
		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
LSB [3 : 0]	0	–180.0	–157.5	–135.0	–112.5	–90.0	–67.5	–45.0	–22.5	+0.0	+22.5	+45.0	+67.5	+90.0	+112.5	+135.0	+157.5
	1	–178.6	–156.1	–133.6	–111.1	–88.6	–66.1	–43.6	–21.1	+1.4	+23.9	+46.4	+68.9	+91.4	+113.9	+136.4	+158.9
	2	–177.2	–154.7	–132.2	–109.7	–87.2	–64.7	–42.2	–19.7	+2.8	+25.3	+47.8	+70.3	+92.8	+115.3	+137.8	+160.3
	3	–175.8	–153.3	–130.8	–108.3	–85.8	–63.3	–40.8	–18.3	+4.2	+26.7	+49.2	+71.7	+94.2	+116.7	+139.2	+161.7
	4	–174.4	–151.9	–129.4	–106.9	–84.4	–61.9	–39.4	–16.9	+5.6	+28.1	+50.6	+73.1	+95.6	+118.1	+140.6	+163.1
	5	–173.0	–150.5	–128.0	–105.5	–83.0	–60.5	–38.0	–15.5	+7.0	+29.5	+52.0	+74.5	+97.0	+119.5	+142.0	+164.5
	6	–171.6	–149.1	–126.6	–104.1	–81.6	–59.1	–36.6	–14.1	+8.4	+30.9	+53.4	+75.9	+98.4	+120.9	+143.4	+165.9
	7	–170.2	–147.7	–125.2	–102.7	–80.2	–57.7	–35.2	–12.7	+9.8	+32.3	+54.8	+77.3	+99.8	+122.3	+144.8	+167.3
	8	–168.8	–146.3	–123.8	–101.3	–78.8	–56.3	–33.8	–11.3	+11.3	+33.8	+56.3	+78.8	+101.3	+123.8	+146.3	+168.8
	9	–167.3	–144.8	–122.3	–99.8	–77.3	–54.8	–32.3	–9.8	+12.7	+35.2	+57.7	+80.2	+102.7	+125.2	+147.7	+170.2
	A	–165.9	–143.4	–120.9	–98.4	–75.9	–53.4	–30.9	–8.4	+14.1	+36.6	+59.1	+81.6	+104.1	+126.6	+149.1	+171.6
	B	–164.5	–142.0	–119.5	–97.0	–74.5	–52.0	–29.5	–7.0	+15.5	+38.0	+60.5	+83.0	+105.5	+128.0	+150.5	+173.0
	C	–163.1	–140.6	–118.1	–95.6	–73.1	–50.6	–28.1	–5.6	+16.9	+39.4	+61.9	+84.4	+106.9	+129.4	+151.9	+174.4
	D	–161.7.	–139.2	–116.7	–94.2	–71.7	–49.2	–26.7	–4.2	+18.3	+40.8	+63.3	+85.8	+108.3	+130.8	+153.3	+175.8
	E	–160.3	–137.8	–115.3	–92.8	–70.3	–47.8	–25.3	–2.8	+19.7	+42.2	+64.7	+87.2	+109.7	+132.2	+154.7	+177.2
	F	–158.9	–136.4	–113.9	–91.4	–68.9	–46.4	–23.9	–1.4	+21.1	+43.6	+66.1	+88.6	+111.1	+133.6	+156.1	+178.6

Filter Characteristics

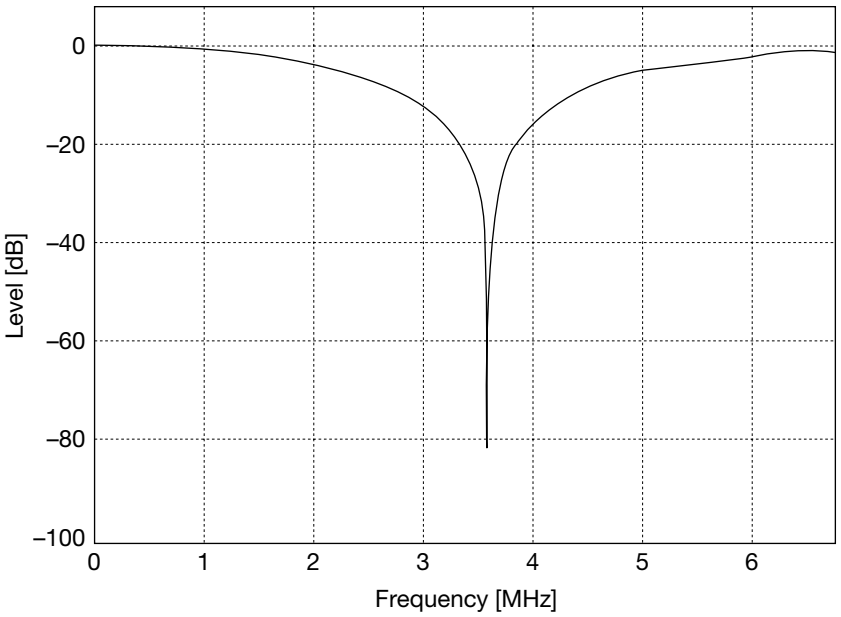
Band Pass Filter (NTSC ITU-R601)



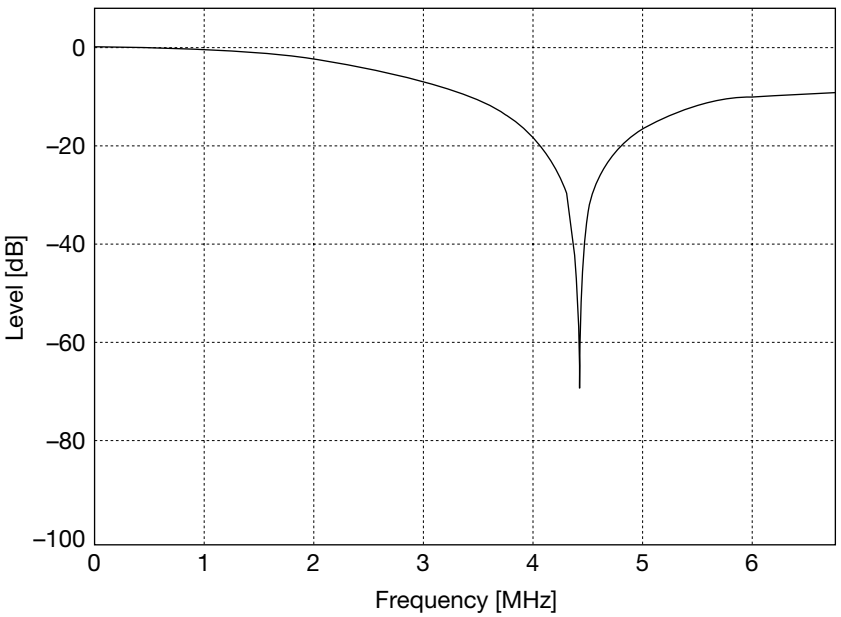
Band Pass Filter (PAL ITU-R601)



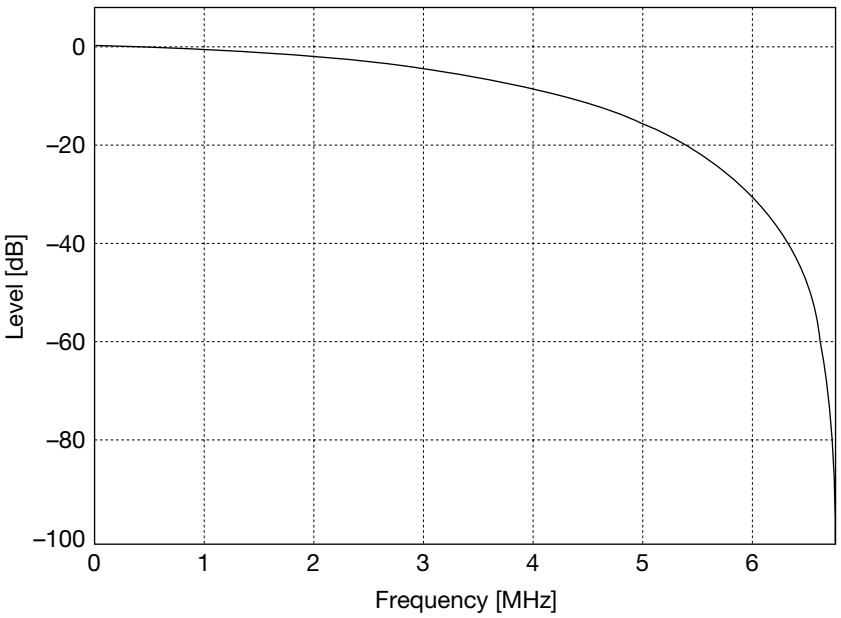
Trap Filter (NTSC ITU-R601)



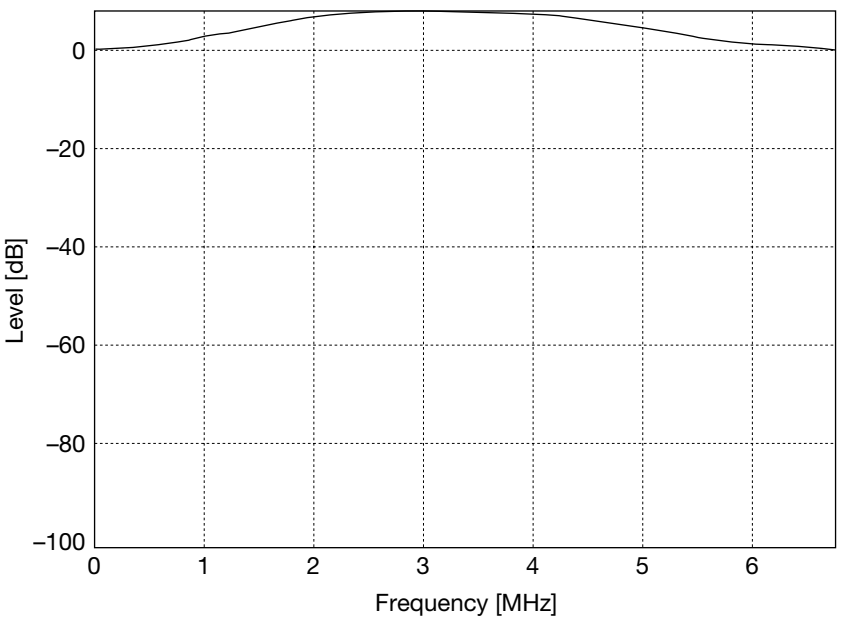
Trap Filter (PAL ITU-R601)



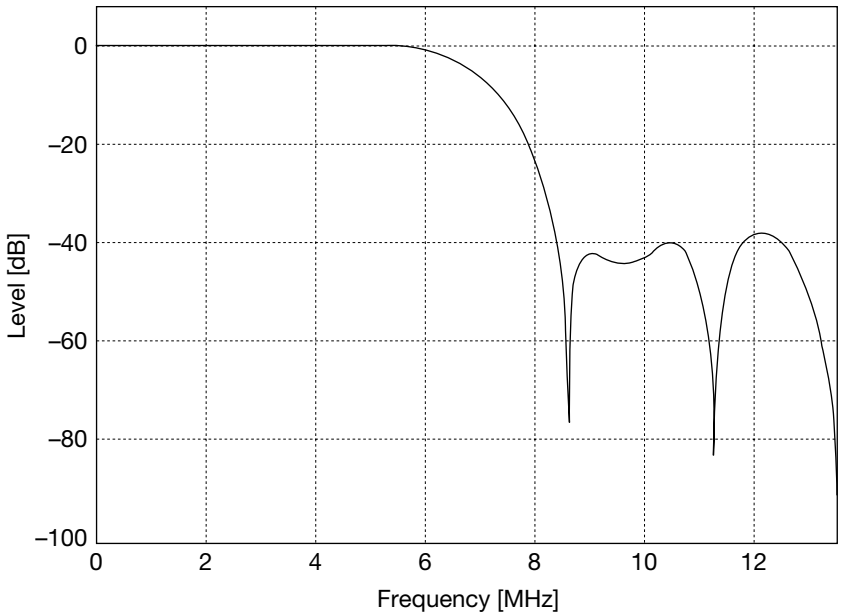
Pre Filter



Sharp Filter

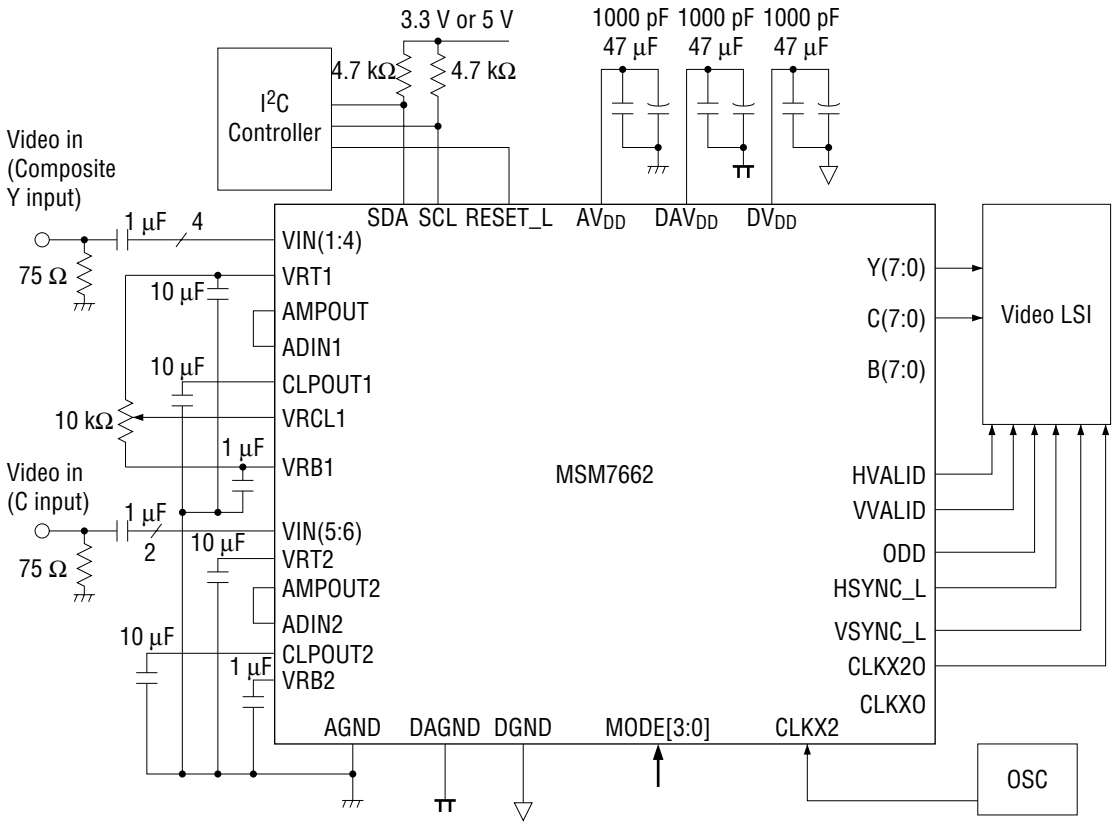


Decimation Filter



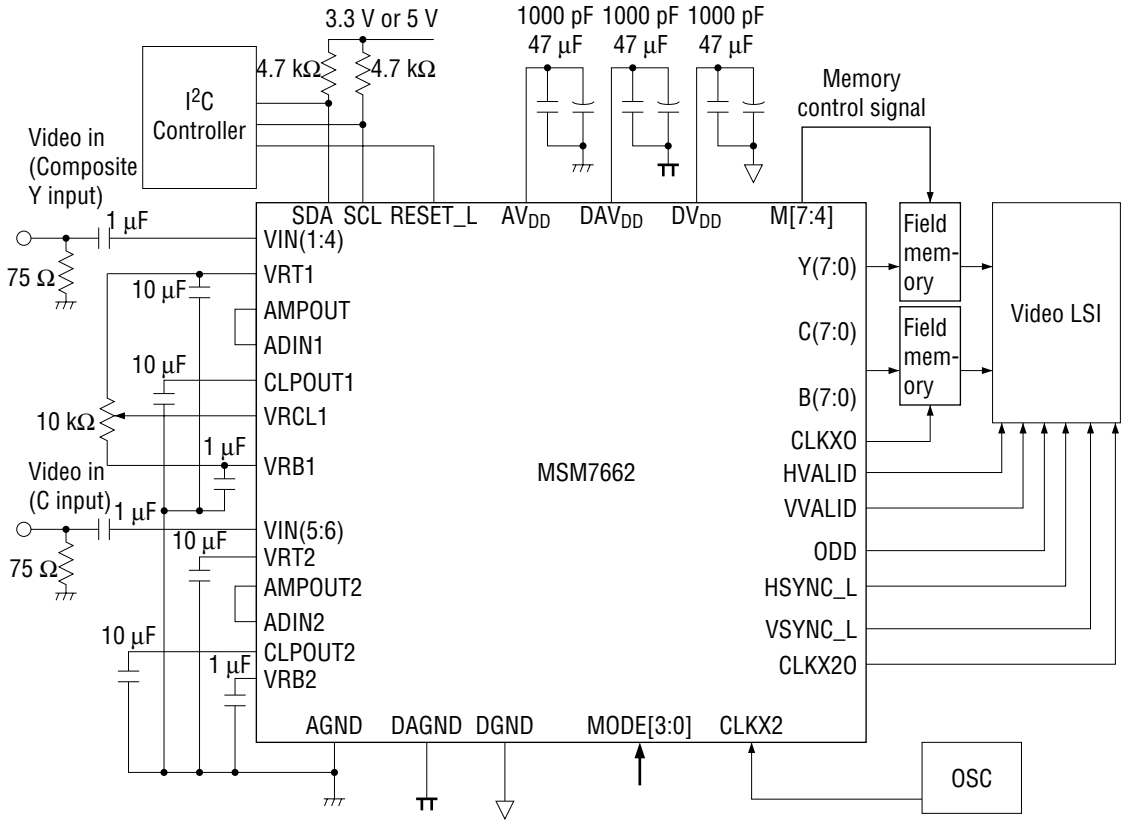
BASIC APPLICATION CIRCUIT EXAMPLES

1) Application Circuit for FIFO-1 and FIFO-2 Modes



- Connect the M7662 decoder and a video LSI device according to the output interface (ITU-R656, 8-bit [YCbCr], 16-bit [YCbCr], RGB).
- Video input can be five composite inputs or two S-Video inputs.
- Connect unused video input pins to AGND. If a composite signal is input, the C input side (video amp, A/D converter, etc.) will be in the OFF operation state.
- If the input is limited by the composite signal, connect VIN (5:6), VRT2, VRB2, AMPOUT2, ADIN2, and CLPOUT2 pins to AGND. Externally attached components such as capacitors may be removed.
- Set the MODE[3:0] pins to the prescribed setting.
- Supply power and GND for analog, A/D, and digital circuits on the circuit board should be separated at the power source wherever possible. Power and GND lines for analog and A/D circuits must be wide and low impedance.

2) Application Circuit for FM-1 and FM-2 Modes

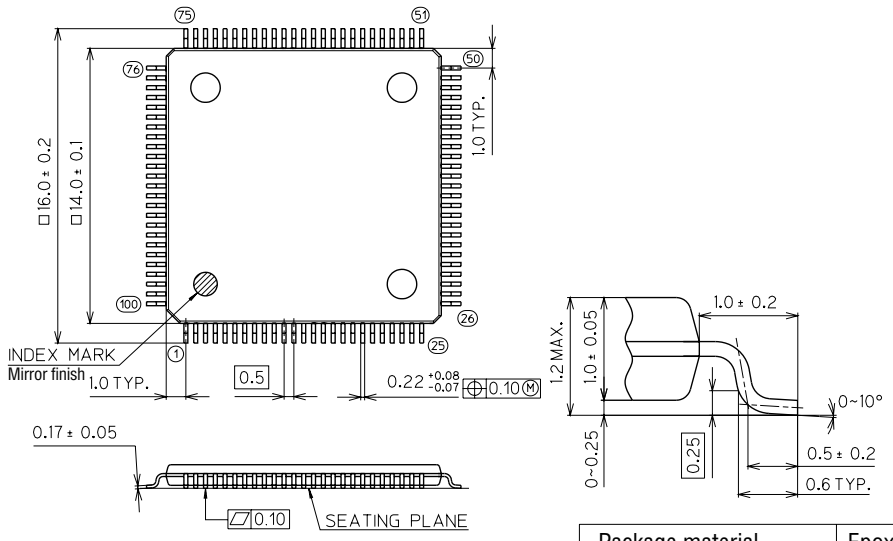


- Select either 16-bit [YCbCr] or RGB output as the output interface.
- Number of field memories utilized
  16-bit [YCbCr]: Use 2 field memories.
  RGB: Use 3 field memories.
- Video input can be five composite inputs or two S-Video inputs.
- Connect unused video input pins to AGND. If a composite signal is input, the C input side (video amp, A/D converter, etc.) will be in the OFF operation state.
- If the input is limited by the composite signal, connect VIN (5:6), VRT2, VRB2, AMPOUT2, ADIN2, and CLPOUT2 pins to AGND. Externally attached components such as capacitors may be removed.
- Set the MODE[3:0] pins to the prescribed setting.
- For the MF-1 mode setting, externally generate and supply control signals for the field memory.
- For the MF-2 mode setting, memory control signals from M[7:4] can be supplied to the field memory.
- For the MF-2 mode setting, the output timing for HSYNC_L, VSYNC_L, ODD, VVALID, and HVALID becomes the memory read timing. Data output from memory is aligned with the variout sync signal timings. (See page 24 and page 25)
- Supply power and GND for analog, A/D, and digital circuits on the circuit board should be separated at the power source wherever possible. Power and GND lines for analog and A/D circuits must be wide and low impedance.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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