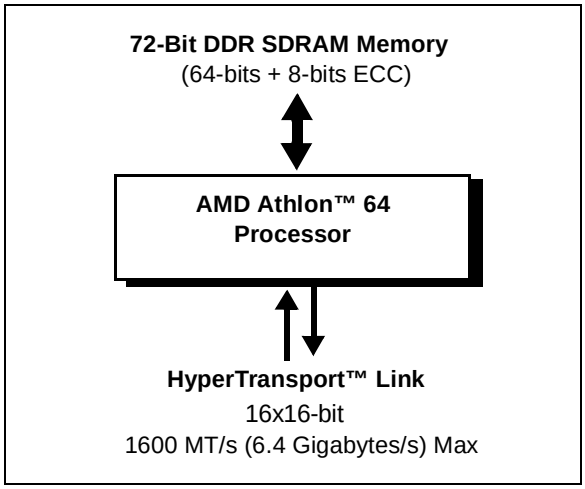
AMD Athlon™ 64 Processor

Data Sheet

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on-chip
- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight new 64-bit integer registers (16 total)
  - Eight new 128-bit SSE/SSE2 registers (16 total)
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 72-bit DDR SDRAM at 100, 133, 166, and 200 MHz
  - Supports up to four registered DIMMs or up to three unbuffered DIMMs
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture—storage in addition to L1 caches
  - 256-Kbyte, 512-Kbyte, and 1-Mbyte options
- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI compliant, including support for processor performance states



- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-like differential, unidirectional
  - DDR SDRAM: SSTL_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
  - 754-pin micro PGA, lidded
  - 1.27-mm pin pitch
  - 29x29 row pin array
  - 40mm x 40mm organic substrate
  - Organic C4 die attach

Publication #	**24659**	Revision:	**3.05**
Issue Date:	**February 2004**		

Trademarks

AMD, the AMD Arrow logo, AMD Athlon, AMD Opteron and combinations thereof, and 3DNow! are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Disclaimer

The contents of this document are provided in connection with Advanced Micro Devices, Inc. ("AMD") products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD's Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD's product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

Contents

List of Figures

List of Tables

Revision History

Date	Revision	Description
February 2004	3.05	Updated TDO and DBRDY pull-up info in Table 29. Updated notes in Table 29 to clarify termination usage. Added PWROK clarification in the Sequencing Relationships section 7.8.3.1. Changed ref from 2.5V to VDDIO in Table 6. Updated note to require VTT tracking VDDIO/2 for Table 33. Updated note for VDDIO to VTT stress during power up/down for Table 33. Added external clock buffer P-state transition restriction recommendation to section 2.4.1.2 and section 3.3. Added 2T DRAM timing description to section 2.4.2.2. Added CLKIN jitter specification to Table 26. Clarified supported HT speeds in section 2.4.1.2. Clarified power supply relationship note for Table 33. Separated and revised VID Voh paramter in Table 19. Revised VDD specifications in Table 32. Storage temp change in Table 15. Clarified external clock buffer P-state transition restriction in section 2.4.2.1. Revised CLKIN jitter typ specification in Table 26. Moved DIMM speed/loading table out of this document. Removed other references to DIMM loading capabilities.
August 2003	3.00	Initial public release.

1 AMD Athlon™ 64 Processor Overview

The AMD Athlon™ 64 processor is designed to support performance desktop and workstation applications. It provides a high-performance HyperTransport™ link to I/O, as well as a single 64-bit high-performance DDR SDRAM memory controller. A block diagram of the AMD Athlon 64 processor is shown in Figure 1.

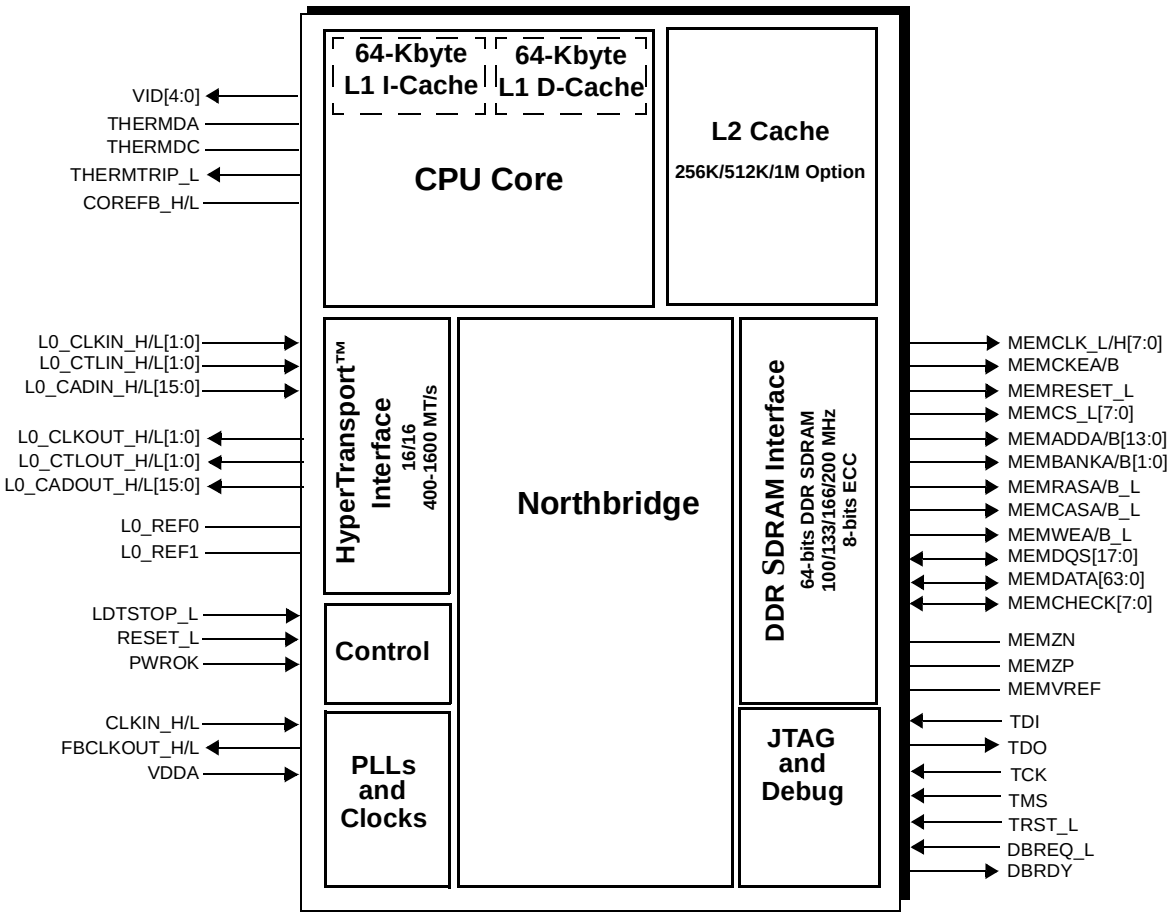


Figure 1. AMD Athlon™ 64 Processor Block Diagram

2 Functional Description

2.1 Instruction Set Support

The AMD Athlon™ 64 processor supports the standard x86-instruction set defined in the *AMD64 Architecture Programmer's Manual*, volumes 3–5, order# 24594. The processor also supports the following extensions to the standard x86 instruction set, which are described in the same volume set:

- AMD64 instructions
- MMX™ and 3DNow!™ technology instructions
- SSE and SSE2 instructions

2.2 Internal Cache Structures

The AMD Athlon 64 processor implements internal caching structures as described in the following sections.

2.2.1 Level 1 Caches

The L1 data cache (L1 D-Cache) contains 64 Kbytes of storage organized as 2-way set associative. The L1 data cache is protected with ECC. Two simultaneous 64-bit operations (load, store or combination) are supported. The L1 instruction cache (L1 I-Cache) contains 64 Kbytes of storage organized as 2-way associative. The L1 Instruction Cache is protected with parity.

2.2.2 Level 2 Cache

The L2 cache contains both instruction and data stream information. It is organized as 16-way set-associative. The L2 cache data and tag store is protected with ECC. When a given cache line in the L2 cache contains instruction stream information, the ECC bits associated with the given line are used to store predecode and branch prediction information.

2.3 Error Handling (Machine Check)

The AMD Athlon 64 processor implements the standard x86 machine check architecture as defined in the *AMD64 Architecture Programmer's Manual, Volume 2*, order# 24593, and the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094.

The machine check architecture is defined with ECC single-bit detection/correction and double-bit detection for the following arrays:

- L1 Data Cache Storage
- L2 Data Cache Storage
- L2 Data Cache Tag
- Instruction Cache
- DRAM (see “Memory Controller” on page 12).

2.4 Northbridge

The Northbridge logic in the AMD Athlon 64 processor refers to the HyperTransport™ technology interface, the memory controller, and their respective interfaces to the CPU core. These interfaces are described in more detail in the following sections.

2.4.1 HyperTransport™ Technology Overview

The AMD Athlon 64 processor includes a 16-bit HyperTransport technology interface designed to be capable of operating up to 1600 mega-transfers per second (MT/s) with a resulting bandwidth of up to 6.4 Gbytes/s (3.2 Gbytes/s in each direction). The processor supports HyperTransport synchronous clocking mode. Refer to the *HyperTransport™ I/O Link Specification* (www.hypertransport.org) for details of link operation.

2.4.1.1 Link Initialization

The HyperTransport technology interface of the AMD Athlon 64 processor can be operated as a single 16-bit link The *HyperTransport™ I/O Link Specification* details the negotiation that occurs at power-on to determine the widths and rates that will be used with the link. Refer also to the *BIOS and Kernel Developer’s Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for information about link initialization and setup of routing tables.

The unused CTLIN_H/L[1] pins must be terminated as follows:

- CTLIN_H[1] must be pulled High.
- CTLIN_L[1] must be pulled Low.

Refer to the *AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details on the proper HyperTransport technology signal termination resistor values.

2.4.1.2 HyperTransport™ Technology Transfer Speeds

The HyperTransport link of the AMD Athlon 64 processor is capable of operating at 200, 400, 600, and 800 MHz (400, 800, 1200, and 1600 MT/s respectively). The link transfer rate is determined during the software configuration of the system, as specified in the *HyperTransport™ I/O Link*

Specification. The maximum transfer rate and bandwidth for the processor's HyperTransport technology interface 1600 MT/s, with a maximum bandwidth of 6.4 Gbytes/s (3.2 Gbytes/s in each direction).

2.4.2 Memory Controller

The processor's memory controller provides a programmable interface to a variety of standard DDR SDRAM DIMM configurations. The following features are supported:

- Self-Refresh mode
- Unbuffered and registered DIMMs with a 64-bit data bus with optional 8 bits of Error Correcting Code (ECC) in one of the following two configurations:
  - — Up to three unbuffered DIMMs according to the loading described in the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094.
  - — Up to four registered DIMMs (note DDR400 not available on registered DIMMs)
- The controller provides programmable control of DRAM timing parameters to support the following memory speeds:
  - — 100-MHz (DDR200) PC-1600 DIMMs
  - — 133-MHz (DDR266) PC-2100 DIMMs
  - — 166-MHz (DDR333) PC-2700 DIMMs
  - — 200-MHz (DDR400) PC-3200 DIMMs (unbuffered DIMMs only)
- DRAM devices that are 4, 8 and 16 bits wide.
- DIMM sizes from 32 Mbytes (using 64Mb x16 DRAMs) to 4Gbyte (using a stacked, registered DIMM with 1Gb x4 DRAMs).
- Interleaving memory within DIMMs.
- Stacked registered DIMMs
- ECC checking with double-bit detect with single-bit correct.
- May be configured for 32-byte or 64-byte burst length.
- Programmable page-policy:
  - — Supports up to sixteen open pages total across all chip-selects.
  - — Statically idle open-page time.
  - — Optional dynamic precharge control based on page-hit/miss history.

For programming information and specific details of these features, refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094.

2.4.2.1 Memory Pin Interface

The memory controller of the AMD Athlon 64 processor supports both registered and unbuffered DDR SDRAM DIMMs. The following list summarizes the differences in the pin interface between registered and unbuffered DIMMs:

- The MEMRESET_L pin is required only for registered DIMMs and is used to reset the register as required to support the Suspend-to-RAM power management state (ACPI S3).
- Registered DIMMS present less loading than unbuffered DIMMs. Therefore, the processor's memory controller supports up to four registered DIMMs or up to three unbuffered DIMMs. Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for restrictions on support for three unbuffered DIMMs.
- A fully populated registered DIMM configuration requires only four differential clock pairs
- An unbuffered 2 DIMM configuration requires up to six differential clock pairs, an unbuffered 3 DIMM configuration requires up to nine clock pairs. Since AMD Athlon™ 64 provides only six clock pairs for unbuffered configurations, the use of an external clock buffer is recommended. The use of processor performance state (P-state) transitions is not recommended when an external clock buffer is used for 3 DIMM clock pair distribution as unpredictable results may occur.
- Registered DIMMs configured with x4 DRAMs require an additional eight DQS pins without ECC support or nine DQS pins with ECC support. The processor's memory controller provides a total of 18 DQS pins to accommodate this requirement. The additional DQS pins can be connected to the DIMMs' Data Mask (DM) pins when connected to x8 or x16 DIMMs. DIMMs populated with x4 devices normally connect the DRAM's Data Mask (DM) pins to VSS. The DM pins are used for partial write support when connected to x8 or x16 devices.
- Registered DIMMs connect only to the 'A' copy of the memory address and command signals

Some processor pin names have 'A' and 'B' suffixes. This is a way to distinguish between two otherwise functionally identical pins that exist as multiple redundant pins to accommodate loading. This is normally the case for address and control pins in unbuffered systems. MEMBANKB[1:0] and MEMADDB[13:0] are different in that they are not logically redundant with their 'A' signal counterparts. During precharges, activates, reads and writes, MEMBANKB[1:0] is logically inverted from MEMBANKA[1:0], and MEMADDB[13:0] is inverted from MEMADDA[13:0] except for bit 10 (which is the auto-precharge bit). In other words, whenever these pins are acting as addresses, they are inverted to minimize switching noise on the motherboard. An example of when they are not inverted would be during initialization when these wires carry data for the Mode Register Set commands.

2.4.2.2 DRAM Operation

At power on reset, the MEMCKEA/B and MEMRESET_L pins are driven low while the processor PLLs are ramping. Clocks are driven on the MEMCLK_H/L7:0] pins only after BIOS programs the appropriate clock ratio value in the memory controller configuration registers. The actual DRAM frequency may vary for some speeds based on the CPU clock multiplier, as shown in Table 1 on page 14 (the memory controller automatically adjusts refresh counters at all speeds as required to

meet the device refresh specifications). Refer to “Power-Up Signal Sequencing” on page 59 for further details on the sequencing of the MEMRESET_L and MEMCKEA/B pins.

Table 1. DRAM Interface Speed vs. CPU Core Clock Multiplier

Multiplier	Core Frequency	DRAM Frequency			
		100 MHz	133 MHz	166 MHz	200 MHz
4	800 MHz	100.00	133.33	160.00	160.00
5	1000 MHz	100.00	125.00	166.66	200.00
6	1200 MHz	100.00	133.33	150.00	200.00
7	1400 MHz	100.00	127.27	155.55	200.00
8	1600 MHz	100.00	133.33	160.00	200.00
9	1800 MHz	100.00	128.57	163.63	200.00
10	2000 MHz	100.00	133.33	166.66	200.00
11	2200 MHz	100.00	129.41	157.14	200.00
12	2400 MHz	100.00	133.33	160.00	200.00
13	2600 MHz	100.00	130.00	162.50	200.00

Table 2 on page 15 lists the maximum memory sizes per chip-select for the various supported DRAM device configurations. Note that for DIMMs using two chip-selects, the total memory size per DIMM is doubled. Refer to the *AMD Athlon™ 64 Processor Motherboard Design Guide*, order #24665 for details on the connection scheme for unbuffered and registered DIMMs in an AMD Athlon 64 processor system.

The use of 2T timing allows support of many DIMM combinations at the maximum DDR speeds listed in Table 1. The 2T timing feature causes commands and addresses to be driven for two clock cycles and qualified with an associated chip select on the second clock cycle, allowing an extra clock of setup to accommodate heavy DIMM loading (such as double-rank DIMMs). Refer to the *BIOS and Kernel Developer’s Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for the DIMM combinations that require 2T timing to operate at the full DRAM speed. 2T timing is supported in CG and later silicon revisions. Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order #30430, for silicon revision determination.

Table 2. Total Memory Sizes Per Chip Select

Devices Used on DIMMs	Size Per CS	Comments
64 M-bit (4M x4-bits x4 banks)	128 Mbyte	Registered DIMMS only
64 M-bit (2M x8-bits x4 banks)	64 Mbyte	
64 M-bit (1M x16-bits x4 banks)	32 Mbyte	
128 M-bit (8M x4-bits x4 banks)	256 Mbyte	Registered DIMMs only
128 M-bit (4M x8-bits x4 banks)	128 Mbyte	
128 M-bit (2M x16-bits x4 banks)	64 Mbyte	
256 M-bit (16M x4-bits x4 banks)	512 Mbyte	Registered DIMMs only
256 M-bit (8M x8-bits x4 banks)	256 Mbyte	
256 M-bit (4M x16-bits x4 banks)	128 Mbyte	
512 M-bit (32M x4-bits x4 banks)	1 Gbyte	Registered DIMMs only
512 M-bit (16M x8-bits x4 banks)	512 Mbyte	
512 M-bit (8M x16-bits x4 banks)	256 Mbyte	
1 G-bit (64M x4-bits x4 banks)	2 Gbyte	Registered DIMMs only
1 G-bit (32M x8-bits x4 banks)	1 Gbyte	
1 G-bit (16M x16-bits x4 banks)	512 Mbyte	

Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for supported DRAM speeds under specific loading conditions.

The controller supports programmable timing and refresh as described in the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094. Auto-refresh is supported and is staggered by t_{RFC} across chip-selects to reduce system noise. Unpopulated DIMM slots are not refreshed.

2.4.2.3 DRAM Power Management

The memory controller supports self-refresh mode to accommodate various power management states such as ACPI C3, S1, and S3 states. The MEMRESET_L pin is provided for resetting the registers on registered DDR SDRAM DIMMs as required for the S3 (Suspend to RAM) power management state.

2.4.2.4 Main Memory Hardware Scrubbing

The memory controller scrubs the main memory arrays to prevent the build up of soft errors. Any correctable or non-correctable errors are logged to the machine check logs and can be programmed to

invoke the machine check interrupt. The scrubbing function can be used in three modes as described in the following sections.

2.4.2.4.1 Sequential Scrubbing

In this mode, the scrubber sequentially proceeds through main memory, performing a read-write cycle or a read-modify-write cycle if a correctable error is found. The scrubber scrubs one cache line on each scrub interval that is programmable from 40 ns to 84 ms.

2.4.2.4.2 Source Correction Scrubbing

In this mode, the scrubber is directed to scrub any cache line that is the source of any corrected error during normal accesses. During normal operation when source correction scrubbing is disabled, single-bit errors are corrected on the fly and the corrected data is passed without updating the source memory location. When source scrubbing is enabled the scrubber also corrects the source memory location.

2.4.2.4.3 Sequential Plus Source Correction Scrubbing

When both sequential and source correction scrubbing are enabled, the scrubber sequentially proceeds through main memory. If a correctable error is detected during normal operation, the scrubber is redirected to the location of the error, and after it corrects that location in main memory it resumes sequential scrubbing at the previous location

3 Power Management

The AMD Athlon™ 64 processor provides the following power management features designed to be compliant with the Advanced Configuration and Power Interface (ACPI) Specification and HyperTransport™ technology:

- Halt state with associated programmable power savings
- STPCLK/Stop Grant protocol capable of supporting eight distinct versions of Stop Grant
- LDTSTOP_L signal support
- Memory controller and host bridge power management
- Processor Performance state (P-State) transition support
- Voltage plane isolation based upon PWROK signal
- Low-power state while RESET_L signal is asserted
- On-die thermal diode

Table 3 maps processor capabilities to ACPI states.

Table 3. Processor Capabilities Mapped to ACPI States

ACPI State	Processor
Processor P-States	Processor P-state transitions are supported on some versions of the processor.
C1	Halt
C2	Stop Grant
Passive Cooling	Passive Cooling is supported by Stop Grant (throttling) and/or P-state transitions.
C3, S1	Stop Grant. In response to LDTSTOP_L assertion, memory is placed in self-refresh mode and the host bridge and memory controller are placed into a low-power state.
S3	Processor core and HyperTransport™ technology voltage planes are not powered. DDR SDRAM interface remains powered and holds memory in self-refresh mode.
S4, S5, G3	All power is removed from the processor.

3.1 Halt

When the HLT instruction is executed, the processor stops program execution and issues a Halt special cycle. The power savings associated with the Halt state are determined by configuration registers in the processor (refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for details of these configuration registers). The CPU clock grid frequency can be divided down in the absence of probe activity that would force the processor's caches to be snooped.

The CPU clock grid is automatically brought to full frequency when probe activity is present and returned to the low-power state when probe activity ceases.

If a STPCLK assertion message is received while the processor is in the Halt State, the processor enters the Stop Grant state and issues a Stop Grant special cycle. When a STPCLK deassertion message is received, the processor exits the Stop Grant state and returns to the Halt State.

The processor exits the Halt State in response to PWROK deassertion, RESET_L assertion, INIT, NMI, SMI, or any unmasked interrupt received over the HyperTransport link.

3.2 STPCLK/Stop Grant

When the processor recognizes the STPCLK assertion message, it enters the Stop Grant state on the next instruction boundary and issues a Stop Grant special cycle. The power savings associated with the Stop Grant state is determined by configuration registers in the processor. The power savings mechanisms associated with the Stop Grant state include the following:

- CPU clock grid divisor applied in the absence of probe activity. If probe activity that requires a cache snoop occurs while the processor is in the Stop Grant state, the clock grid is ramped back up to service the probe. When probe activity ceases, the CPU clock grid is ramped back down again.
- Placing system memory into self-refresh mode in response to LDTSTOP_L signal assertion.
- Ramping the processor host bridge/memory controller clock grid down in response to LDTSTOP_L signal assertion.
- Processor performance state transition in response to LDTSTOP_L signal assertion.
- Changing HyperTransport link width and/or link frequency in response to LDTSTOP_L signal assertion.

The processor exits the Stop Grant state when it receives the following:

- A STPCLK deassertion message.
- RESET_L pin asserted, or an INIT assertion message.
- PWROK is deasserted.

If the LDTSTOP_L signal is asserted after the processor is in the Stop Grant state, then LDTSTOP_L must be deasserted, and the HyperTransport link must be re-initialized before a STPCLK deassertion message can be received by the processor to bring the processor out of the Stop Grant state.

The processor's host bridge ensures that STPCLK messages are passed to the CPU prior to the subsequent I/O response to the cycle that caused STPCLK assertion, as long as the subsequent I/O response message has the PassPW bit clear and the Unit ID of the response matches the Unit ID of the STPCLK message.

3.3 Processor Performance State Transitions

Some versions of the AMD Athlon 64 processor support processor performance state (P-State) transitions. The use of P-state transitions is not recommended when an external clock buffer is used for 3 DIMM clock pair distribution as unpredictable results may occur. Processor P-States are valid combinations of processor voltage and frequency. P-State transitions are performed through the FID_Change protocol. The processor provides two Model-Specific Registers (MSRs) in support of the FID_Change protocol: the FIDVID_CTL and FIDVID_STATUS MSRs. The FIDVID_CTL MSR allows software to dictate what P-State the processor will transition to, and to initiate the transition to that state. The FIDVID_STATUS MSR allows software to determine when a P-State transition is complete.

P-state transitions are comprised of multiple FID only and VID only transitions as described in *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094. Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet*, order# 30430 for a list of the valid P-States for this processor.

During VID only transitions, no HyperTransport FIDVID_Change system management message is issued when the processor's FIDVID_CTL MSR's FidVidChangeInitiate bit is set. The processor is not put into Stop Grant, but rather drives the new VID while the processor continues to execute instructions.

The following describes a FID only transition:

- When the processor's FIDVID_CTL MSR's FidVidChangeInitiate bit is set, the processor issues a FID_Change special cycle.
- When the processor subsequently receives a STPCLK message, it enters the Stop Grant state and issues a Stop Grant special cycle with a System Management Action Field (SMAF, bits 3:1 of the system management command field) corresponding to the SMAF received with the STPCLK message.

Note: *If two STPCLK messages are issued before the processor issues a Stop Grant special cycle, the SMAF issued will correspond to the last STPCLK message received.*

- When the processor's host bridge broadcasts the Stop Grant special cycle with a SMAF indicating FID/VID change down its HyperTransport link(s), the processor is primed to transition its core frequency or core voltage in response to LDTSTOP_L assertion.

- When the LDTSTOP_L pin is asserted, the processor performs the following steps:
  - — Disconnects its HyperTransport link(s)
  - — Places system memory into self-refresh mode
  - — Ramps its entire clock grid, including host bridge and memory controller, down by a programmable value
  - — Transitions its core frequency
- When the frequency transition is complete and LDTSTOP_L is deasserted, the processor performs the following steps:
  - — Ramps its host bridge and memory controller clock grid back up to full frequency
  - — Brings system memory out of self-refresh mode
  - — Reconnects its HyperTransport link(s)
- When a STPCLK deassertion message is received, the CPU clock grid is ramped up to full operating frequency, and the processor exits the Stop Grant state.

Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for the detailed P-state transition algorithm. Refer to the *AMD Athlon™ 64 Power and Thermal Data Sheet*, order# 30430, to determine support for processor P-state transitions.

3.4 PWROK

When PWROK is deasserted, the processor performs the following steps:

- Isolates its VDDIO- and VTT-powered logic from all other internal logic to prevent leakage current paths between power planes.
- Tristates all DDR SDRAM I/O pins except for the MEMCKEA/B and MEMRESET_L outputs, which are driven Low.
- Drives its VID[4:0] outputs to the value that selects the startup core voltage level.

3.5 RESET_L and MEMRESET_L

When RESET_L is asserted, the processor performs the following steps:

- The processor core is held in a low-power state.
- The MEMCKEA/B and MEMRESET_L outputs are forced Low.

After RESET_L is deasserted, BIOS must program the appropriate clock divisor in the memory controller configuration registers, causing the MEMCLK_H/L[7:0] clocks to be driven. Refer to "Power-Up Signal Sequencing" on page 59 for details of RESET_L and MEMRESET_L sequencing during initial power-on.

3.6 Thermal Diode

The processor provides an on-die thermal diode with anode and cathode brought out to processor pins. This diode can be read by an external temperature sensor to determine the processor's temperature. Refer to the *AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details on connecting the thermal diode.

3.7 THERMTRIP_L

The AMD Athlon 64 processor provides a hardware-enforced thermal protection mechanism. When the processor's die temperature exceeds a specified temperature, the processor is designed to stop its internal clocks and assert the THERMTRIP_L output.

THERMTRIP_L assertion is only valid when PWROK is asserted and RESET_L is deasserted.

If the processor's die temperature still exceeds the thermal trip point when RESET_L is deasserted, THERMTRIP_L will immediately be reasserted and the processor's internal clocks will be stopped.

THERMTRIP_L assertion indicates the processor die temperature has exceeded normal operating parameters. PWROK must be deasserted in response to a THERMTRIP_L assertion to enable proper processor operation.

4 Connection Diagrams

The pinout for the AMD Athlon™ 64 processor is illustrated in this chapter, and is divided into two parts. Figure 2 on page 23 shows the left-hand side of the top view, which is the DDR SDRAM interface. Figure 3 on page 24 shows the right-hand side of the top view, the HyperTransport™ technology interface.

The pin designations are defined in Chapter 5. Table 4 on page 26 lists the pins alphabetically by pin name.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			MEMDATA[43]	MEMDATA[46]	MEMDATA[49]	MEMDATA[52]	MEMDQS[15]	MEMDQS[6]	MEMDATA[50]	MEMDATA[55]	MEMDATA[56]	MEMDATA[61]	MEMDQS[16]	MEMDQS[7]	MEMDATA[58]
B		VSS	MEMDATA[42]	VSS	MEMDATA[48]	VSS	NC_B7	VSS	MEMDATA[54]	VSS	MEMDATA[60]	VSS	NC_B13	VSS	MEMDATA[62]
C	NC_C1	MEMDQS[14]	NC_C3	MEMCS_L[1]	MEMDATA[47]	NC_C6	MEMDATA[53]	MEMCS_L[6]	NC_C9	MEMCLK_L[7]	MEMDATA[51]	NC_C12	MEMDATA[57]	MEMZP	NC_C15
D	MEMDQS[5]	VSS	NC_D3	MEMCASA_L	VDDIO	MEMCS_L[3]	VDDIO	MEMCS_L[7]	VDDIO	MEMCLK_H[7]	VDDIO	NC_D12	VDDIO	MEMZN	VDDIO
E	MEMDATA[44]	MEMDATA[45]	MEMDATA[41]	VDDIO	MEMCS_L[0]	MEMCS_L[2]	MEMCS_L[4]	MEMCS_L[5]	MEMADDB[13]	MEMADDA[13]	MEMCLK_L[6]	MEMCLK_H[6]	NC_E13	NC_E14	VSS
F	MEMDATA[40]	VSS	NC_F3	MEMWEB_L	MEMCASB_L	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS
G	MEMDATA[38]	MEMDATA[39]	MEMDATA[35]	VDDIO	MEMWEA_L	VSS	VDDIO	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD
H	MEMDQS[13]	VSS	MEMBANKA[0]	MEMRASB_L	MEMRASA_L	VDDIO	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS
J	MEMDQS[4]	MEMDATA[34]	NC_J3	VDDIO	MEMBANKB[0]	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
K	NC_K1	VSS	MEMBANKA[1]	MEMCLK_L[2]	MEMCLK_H[2]	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
L	MEMDATA[36]	MEMDATA[33]	MEMDATA[37]	VDDIO	MEMBANKB[1]	VSS	VDD	VSS	VDD	VSS					
M	MEMDATA[32]	VSS	MEMADDB[0]	MEMADDB[10]	MEMADDA[10]	VDDIO	VSS	VDD	VSS	VDD					
N	MEMCHECK[6]	MEMCHECK[3]	MEMCHECK[7]	VDDIO	MEMADDA[0]	VSS	VDD	VSS	VDD	VSS					
P	MEMCHECK[2]	VSS	MEMCLK_H[0]	MEMCLK_L[0]	MEMCLK_L[1]	VDDIO	VSS	VDD	VSS	VDD					
R	MEMDQS[17]	NC_R2	NC_R3	VDDIO	MEMCLK_H[1]	VSS	VDD	VSS	VDD	VSS					
T	MEMDQS[8]	VSS	MEMADDA[1]	MEMADDB[1]	MEMADDA[2]	VDDIO	VSS	VDD	VSS	VDD					
U	MEMCHECK[1]	MEMCHECK[0]	MEMCHECK[5]	VDDIO	MEMADDB[2]	VSS	VDD	VSS	VDD	VSS					
V	MEMCHECK[4]	VSS	MEMCLK_H[3]	MEMCLK_L[3]	MEMADDA[3]	VDDIO	VSS	VDD	VSS	VDD					
W	MEMDATA[31]	MEMDATA[27]	MEMDATA[30]	VDDIO	MEMADDB[3]	VSS	VDD	VSS	VDD	VSS					
Y	MEMDATA[26]	VSS	MEMADDA[4]	MEMADDB[4]	MEMADDA[6]	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AA	MEMDQS[12]	NC_AA2	NC_AA3	VDDIO	MEMADDB[6]	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AB	MEMDQS[3]	VSS	MEMADDB[5]	MEMADDA[5]	MEMADDA[8]	VDDIO	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AC	MEMDATA[29]	MEMDATA[25]	MEMDATA[28]	VDDIO	MEMADDB[8]	VSS	VDDIO	VSS	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD
AD	MEMDATA[24]	VSS	MEMADDA[7]	MEMADDB[7]	MEMADDB[9]	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	VSS
AE	MEMDATA[23]	MEMDATA[19]	MEMDATA[22]	VDDIO	MEMADDA[9]	MEMADDA[12]	MEMCKEB	MEMCKEA	NC_AE9	MEMCLK_L[4]	VDDIO_SENSE	VDDIOFB_H	VTT_SENSE	VSS	VID[0]
AF	MEMDATA[18]	VSS	MEMADDA[11]	MEMADDB[11]	VDDIO	MEMADDB[12]	VDDIO	MEMCLK_H[5]	VDDIO	MEMCLK_H[4]	VDDIO	VDDIOFB_L	VDDIO	VID[3]	VID[1]
AG	MEMDQS[11]	NC_AG2	MEMDATA[21]	NC_AG4	MEMDATA[11]	NC_AG6	NC_AG7	MEMCLK_L[5]	NC_AG9	MEMRESET_L	MEMDATA[3]	MEMVREF1	VID[4]	VID[2]	VTT_B
AH	NC_AH1	VSS	MEMDATA[17]	VSS	MEMDATA[10]	VSS	MEMDQS[10]	VSS	MEMDATA[12]	VSS	MEMDATA[7]	VSS	MEMDQS[9]	VSS	MEMDATA[5]
AJ		MEMDQS[2]	MEMDATA[16]	MEMDATA[20]	MEMDATA[15]	MEMDATA[14]	MEMDATA[13]	MEMDQS[1]	MEMDATA[9]	MEMDATA[8]	MEMDATA[6]	MEMDATA[2]	MEMDQS[0]	MEMDATA[1]	MEMDATA[4]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 2. DDR SDRAM Interface—Micro PGA Top View, Left Side

16	17	18	19	20	21	22	23	24	25	26	27	28	29	
MEMDATA[63]	MEMDATA[59]	VTT_A	NC_A19	THERMTRIP_L	TDI	TDO	COREFB_H	COREFB_L	NC_A25	THERMDA	THERMDC	KEY1		A
VSS	VTT_A	NC_B18	NC_B19	VDD	TRST_L	VSS	CORE_SENSE	VDD	VSS	VSS	VLDT0_A	VSS	VLDT0_A	B
VTT_A	VTT_A	NC_C18	NC_C19	NC_C20	NC_C21	NC_C22	NC_C23	NC_C24	VSS	VLDT0_A	VSS	VLDT0_A	VSS	C
VSS	VTT_A	NC_D18	VSS	NC_D20	VSS	NC_D22	VSS	VDD	VLDT0_A	VSS	VLDT0_A	VSS	VLDT0_A	D
VSS	TCK	VSS	VDD	TMS	VDD	VSS	VDD	VSS	L0_CADOUT_H[9]	L0_CADOUT_H[8]	L0_CADOUT_L[8]	VDD	L0_CADOUT_H[0]	E
VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CADOUT_L[9]	VDD	L0_CADOUT_L[1]	L0_CADOUT_H[1]	L0_CADOUT_L[0]	F
VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	L0_CADOUT_H[11]	L0_CADOUT_H[10]	L0_CADOUT_L[10]	VSS	L0_CADOUT_H[2]	G
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CADOUT_L[11]	VSS	L0_CADOUT_L[3]	L0_CADOUT_H[3]	L0_CADOUT_L[2]	H
VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	L0_CADOUT_H[12]	L0_CLKOUT_H[1]	L0_CLKOUT_L[1]	VDD	L0_CLKOUT_H[0]	J
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CADOUT_L[12]	VDD	L0_CADOUT_L[4]	L0_CADOUT_H[4]	L0_CLKOUT_L[0]	K
				VSS	VDD	VSS	VDD	VSS	L0_CADOUT_H[14]	L0_CADOUT_H[13]	L0_CADOUT_L[13]	VSS	L0_CADOUT_H[5]	L
				VDD	VSS	VDD	VSS	VDD	L0_CADOUT_L[14]	VSS	L0_CADOUT_L[6]	L0_CADOUT_H[6]	L0_CADOUT_L[5]	M
				VSS	VDD	VSS	VDD	VSS	L0_CTLOUT_H[1]	L0_CADOUT_H[15]	L0_CADOUT_L[15]	VDD	L0_CADOUT_H[7]	N
				VDD	VSS	VDD	VSS	VDD	L0_CTLOUT_L[1]	VDD	L0_CTLOUT_L[0]	L0_CTLOUT_H[0]	L0_CADOUT_L[7]	P
				VSS	VDD	VSS	VDD	VSS	L0_CADIN_L[15]	L0_CTLIN_L[1]	L0_CTLIN_H[1]	VSS	L0_CTLIN_L[0]	R
				VDD	VSS	VDD	VSS	VDD	L0_CADIN_H[15]	VSS	L0_CADIN_H[7]	L0_CADIN_L[7]	L0_CTLIN_H[0]	T
				VSS	VDD	VSS	VDD	VSS	L0_CADIN_L[13]	L0_CADIN_L[14]	L0_CADIN_H[14]	VDD	L0_CADIN_L[6]	U
				VDD	VSS	VDD	VSS	VDD	L0_CADIN_H[13]	VDD	L0_CADIN_H[5]	L0_CADIN_L[5]	L0_CADIN_H[6]	V
				VSS	VDD	VSS	VDD	VSS	L0_CLKIN_L[1]	L0_CADIN_L[12]	L0_CADIN_H[12]	VSS	L0_CADIN_L[4]	W
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CLKIN_H[1]	VSS	L0_CLKIN_H[0]	L0_CLKIN_L[0]	L0_CADIN_H[4]	Y
VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	L0_CADIN_L[10]	L0_CADIN_L[11]	L0_CADIN_H[11]	VDD	L0_CADIN_L[3]	AA
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CADIN_H[10]	VDD	L0_CADIN_H[2]	L0_CADIN_L[2]	L0_CADIN_H[3]	AB
VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	L0_CADIN_L[8]	L0_CADIN_L[9]	L0_CADIN_H[9]	VSS	L0_CADIN_L[1]	AC
VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L0_CADIN_H[8]	VSS	L0_CADIN_H[0]	L0_CADIN_L[0]	L0_CADIN_H[1]	AD
VSS	VDD	PWROK	DBREQ_L	VSS	NC_AE21	NC_AE22	NC_AE23	NC_AE24	VDD	L0_REF0	VDD	VLDT0_B	VSS	AE
VTT_B	VSS	NC_AF18	VSS	RESET_L	NC_AF21	NC_AF22	NC_AF23	NC_AF24	VLDT0_B	VSS	L0_REF1	VSS	VLDT0_B	AF
VTT_B	NC_AG17	NC_AG18	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VLDT0_B	VSS	VLDT0_B	VSS	AG
VTT_B	DBRDY	NC_AH18	G_FBCLKOUT_H	VSS	CLKIN_L	VSS	NC_AH23	VDD	VDDA1	VSS	VLDT0_B	VSS	VLDT0_B	AH
MEMDATA[0]	VTT_B	NC_AJ18	G_FBCLKOUT_L	VSS	CLKIN_H	VSS	NC_AJ23	VSS	VDDA2	VSS	LDTSTOP_L	KEY0		AJ
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 3. HyperTransport™ Technology Interface—Micro PGA Top View, Right Side

5 Pin Designations

Table 4, beginning on page 26, lists the pins alphabetically by pin name.

Table 4. Pin List by Name

Name	Pin	Name	Pin	Name	Pin
CLKIN_H	AJ21	L0_CADIN_L[15]	R25	L0_CADOUT_L[3]	H27
CLKIN_L	AH21	L0_CADIN_L[2]	AB28	L0_CADOUT_L[4]	K27
CORE_SENSE	B23	L0_CADIN_L[3]	AA29	L0_CADOUT_L[5]	M29
COREFB_H	A23	L0_CADIN_L[4]	W29	L0_CADOUT_L[6]	M27
COREFB_L	A24	L0_CADIN_L[5]	V28	L0_CADOUT_L[7]	P29
DBRDY	AH17	L0_CADIN_L[6]	U29	L0_CADOUT_L[8]	E27
DBREQ_L	AE19	L0_CADIN_L[7]	T28	L0_CADOUT_L[9]	F25
FBCLKOUT_H	AH19	L0_CADIN_L[8]	AC25	L0_CLKIN_H[0]	Y27
FBCLKOUT_L	AJ19	L0_CADIN_L[9]	AC26	L0_CLKIN_H[1]	Y25
KEY0	AJ28	L0_CADOUT_H[0]	E29	L0_CLKIN_L[0]	Y28
KEY1	A28	L0_CADOUT_H[1]	F28	L0_CLKIN_L[1]	W25
L0_CADIN_H[0]	AD27	L0_CADOUT_H[10]	G26	L0_CLKOUT_H[0]	J29
L0_CADIN_H[1]	AD29	L0_CADOUT_H[11]	G25	L0_CLKOUT_H[1]	J26
L0_CADIN_H[10]	AB25	L0_CADOUT_H[12]	J25	L0_CLKOUT_L[0]	K29
L0_CADIN_H[11]	AA27	L0_CADOUT_H[13]	L26	L0_CLKOUT_L[1]	J27
L0_CADIN_H[12]	W27	L0_CADOUT_H[14]	L25	L0_CTLIN_H[0]	T29
L0_CADIN_H[13]	V25	L0_CADOUT_H[15]	N26	L0_CTLIN_H[1]	R27
L0_CADIN_H[14]	U27	L0_CADOUT_H[2]	G29	L0_CTLIN_L[0]	R29
L0_CADIN_H[15]	T25	L0_CADOUT_H[3]	H28	L0_CTLIN_L[1]	R26
L0_CADIN_H[2]	AB27	L0_CADOUT_H[4]	K28	L0_CTLOUT_H[0]	P28
L0_CADIN_H[3]	AB29	L0_CADOUT_H[5]	L29	L0_CTLOUT_H[1]	N25
L0_CADIN_H[4]	Y29	L0_CADOUT_H[6]	M28	L0_CTLOUT_L[0]	P27
L0_CADIN_H[5]	V27	L0_CADOUT_H[7]	N29	L0_CTLOUT_L[1]	P25
L0_CADIN_H[6]	V29	L0_CADOUT_H[8]	E26	L0_REF0	AE26
L0_CADIN_H[7]	T27	L0_CADOUT_H[9]	E25	L0_REF1	AF27
L0_CADIN_H[8]	AD25	L0_CADOUT_L[0]	F29	LDTSTOP_L	AJ27
L0_CADIN_H[9]	AC27	L0_CADOUT_L[1]	F27	MEMADDA[0]	N5
L0_CADIN_L[0]	AD28	L0_CADOUT_L[10]	G27	MEMADDA[1]	T3
L0_CADIN_L[1]	AC29	L0_CADOUT_L[11]	H25	MEMADDA[10]	M5
L0_CADIN_L[10]	AA25	L0_CADOUT_L[12]	K25	MEMADDA[11]	AF3
L0_CADIN_L[11]	AA26	L0_CADOUT_L[13]	L27	MEMADDA[12]	AE6
L0_CADIN_L[12]	W26	L0_CADOUT_L[14]	M25	MEMADDA[13]	E10
L0_CADIN_L[13]	U25	L0_CADOUT_L[15]	N27	MEMADDA[2]	T5
L0_CADIN_L[14]	U26	L0_CADOUT_L[2]	H29	MEMADDA[3]	V5

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
MEMADDA[4]	Y3	MEMCKEA	AE8	MEMDATA[16]	AJ3
MEMADDA[5]	AB4	MEMCKEB	AE7	MEMDATA[17]	AH3
MEMADDA[6]	Y5	MEMCLK_H[0]	P3	MEMDATA[18]	AF1
MEMADDA[7]	AD3	MEMCLK_H[1]	R5	MEMDATA[19]	AE2
MEMADDA[8]	AB5	MEMCLK_H[2]	K5	MEMDATA[2]	AJ12
MEMADDA[9]	AE5	MEMCLK_H[3]	V3	MEMDATA[20]	AJ4
MEMADDB[0]	M3	MEMCLK_H[4]	AF10	MEMDATA[21]	AG3
MEMADDB[1]	T4	MEMCLK_H[5]	AF8	MEMDATA[22]	AE3
MEMADDB[10]	M4	MEMCLK_H[6]	E12	MEMDATA[23]	AE1
MEMADDB[11]	AF4	MEMCLK_H[7]	D10	MEMDATA[24]	AD1
MEMADDB[12]	AF6	MEMCLK_L[0]	P4	MEMDATA[25]	AC2
MEMADDB[13]	E9	MEMCLK_L[1]	P5	MEMDATA[26]	Y1
MEMADDB[2]	U5	MEMCLK_L[2]	K4	MEMDATA[27]	W2
MEMADDB[3]	W5	MEMCLK_L[3]	V4	MEMDATA[28]	AC3
MEMADDB[4]	Y4	MEMCLK_L[4]	AE10	MEMDATA[29]	AC1
MEMADDB[5]	AB3	MEMCLK_L[5]	AG8	MEMDATA[3]	AG11
MEMADDB[6]	AA5	MEMCLK_L[6]	E11	MEMDATA[30]	W3
MEMADDB[7]	AD4	MEMCLK_L[7]	C10	MEMDATA[31]	W1
MEMADDB[8]	AC5	MEMCS_L[0]	E5	MEMDATA[32]	M1
MEMADDB[9]	AD5	MEMCS_L[1]	C4	MEMDATA[33]	L2
MEMBANKA[0]	H3	MEMCS_L[2]	E6	MEMDATA[34]	J2
MEMBANKA[1]	K3	MEMCS_L[3]	D6	MEMDATA[35]	G3
MEMBANKB[0]	J5	MEMCS_L[4]	E7	MEMDATA[36]	L1
MEMBANKB[1]	L5	MEMCS_L[5]	E8	MEMDATA[37]	L3
MEMCASA_L	D4	MEMCS_L[6]	C8	MEMDATA[38]	G1
MEMCASB_L	F5	MEMCS_L[7]	D8	MEMDATA[39]	G2
MEMCHECK[0]	U2	MEMDATA[0]	AJ16	MEMDATA[4]	AJ15
MEMCHECK[1]	U1	MEMDATA[1]	AJ14	MEMDATA[40]	F1
MEMCHECK[2]	P1	MEMDATA[10]	AH5	MEMDATA[41]	E3
MEMCHECK[3]	N2	MEMDATA[11]	AG5	MEMDATA[42]	B3
MEMCHECK[4]	V1	MEMDATA[12]	AH9	MEMDATA[43]	A3
MEMCHECK[5]	U3	MEMDATA[13]	AJ7	MEMDATA[44]	E1
MEMCHECK[6]	N1	MEMDATA[14]	AJ6	MEMDATA[45]	E2
MEMCHECK[7]	N3	MEMDATA[15]	AJ5	MEMDATA[46]	A4

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
MEMDATA[47]	C5	MEMDQS[4]	J1	NC_AG9	AG9
MEMDATA[48]	B5	MEMDQS[5]	D1	NC_AH1	AH1
MEMDATA[49]	A5	MEMDQS[6]	A8	NC_AH18	AH18
MEMDATA[5]	AH15	MEMDQS[7]	A14	NC_AH23	AH23
MEMDATA[50]	A9	MEMDQS[8]	T1	NC_AJ18	AJ18
MEMDATA[51]	C11	MEMDQS[9]	AH13	NC_AJ23	AJ23
MEMDATA[52]	A6	MEMRASA_L	H5	NC_B13	B13
MEMDATA[53]	C7	MEMRASB_L	H4	NC_B18	B18
MEMDATA[54]	B9	MEMRESET_L	AG10	NC_B19	B19
MEMDATA[55]	A10	MEMVREF1	AG12	NC_B7	B7
MEMDATA[56]	A11	MEMWEA_L	G5	NC_C1	C1
MEMDATA[57]	C13	MEMWEB_L	F4	NC_C12	C12
MEMDATA[58]	A15	MEMZN	D14	NC_C15	C15
MEMDATA[59]	A17	MEMZP	C14	NC_C18	C18
MEMDATA[6]	AJ11	NC_A19	A19	NC_C19	C19
MEMDATA[60]	B11	NC_A25	A25	NC_C20	C20
MEMDATA[61]	A12	NC_AA2	AA2	NC_C21	C21
MEMDATA[62]	B15	NC_AA3	AA3	NC_C22	C22
MEMDATA[63]	A16	NC_AE21	AE21	NC_C23	C23
MEMDATA[7]	AH11	NC_AE22	AE22	NC_C24	C24
MEMDATA[8]	AJ10	NC_AE23	AE23	NC_C3	C3
MEMDATA[9]	AJ9	NC_AE24	AE24	NC_C6	C6
MEMDQS[0]	AJ13	NC_AE9	AE9	NC_C9	C9
MEMDQS[1]	AJ8	NC_AF18	AF18	NC_D12	D12
MEMDQS[10]	AH7	NC_AF21	AF21	NC_D18	D18
MEMDQS[11]	AG1	NC_AF22	AF22	NC_D20	D20
MEMDQS[12]	AA1	NC_AF23	AF23	NC_D22	D22
MEMDQS[13]	H1	NC_AF24	AF24	NC_D3	D3
MEMDQS[14]	C2	NC_AG17	AG17	NC_E13	E13
MEMDQS[15]	A7	NC_AG18	AG18	NC_E14	E14
MEMDQS[16]	A13	NC_AG2	AG2	NC_F3	F3
MEMDQS[17]	R1	NC_AG4	AG4	NC_J3	J3
MEMDQS[2]	AJ2	NC_AG6	AG6	NC_K1	K1
MEMDQS[3]	AB1	NC_AG7	AG7	NC_R2	R2

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
NC_R3	R3	VDD	H18	VDD	N21
PWROK	AE18	VDD	H20	VDD	N23
RESET_L	AF20	VDD	H22	VDD	N28
TCK	E17	VDD	H24	VDD	P8
TDI	A21	VDD	J9	VDD	P10
TDO	A22	VDD	J11	VDD	P20
THERMDA	A26	VDD	J13	VDD	P22
THERMDC	A27	VDD	J15	VDD	P24
THERMTRIP_L	A20	VDD	J17	VDD	P26
TMS	E20	VDD	J19	VDD	R7
TRST_L	B21	VDD	J21	VDD	R9
VDD	B20	VDD	J23	VDD	R21
VDD	B24	VDD	J28	VDD	R23
VDD	D24	VDD	K8	VDD	T8
VDD	E19	VDD	K10	VDD	T10
VDD	E21	VDD	K12	VDD	T20
VDD	E23	VDD	K14	VDD	T22
VDD	E28	VDD	K16	VDD	T24
VDD	F18	VDD	K18	VDD	U7
VDD	F20	VDD	K20	VDD	U9
VDD	F22	VDD	K22	VDD	U21
VDD	F24	VDD	K24	VDD	U23
VDD	F26	VDD	K26	VDD	U28
VDD	G11	VDD	L7	VDD	V8
VDD	G13	VDD	L9	VDD	V10
VDD	G15	VDD	L21	VDD	V20
VDD	G17	VDD	L23	VDD	V22
VDD	G19	VDD	M8	VDD	V24
VDD	G21	VDD	M10	VDD	V26
VDD	G23	VDD	M20	VDD	W7
VDD	H10	VDD	M22	VDD	W9
VDD	H12	VDD	M24	VDD	W21
VDD	H14	VDD	N7	VDD	W23
VDD	H16	VDD	N9	VDD	Y8

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
VDD	Y10	VDD	AD20	VDDIO	P6
VDD	Y12	VDD	AD22	VDDIO	R4
VDD	Y14	VDD	AD24	VDDIO	T6
VDD	Y16	VDD	AE17	VDDIO	U4
VDD	Y18	VDD	AE25	VDDIO	V6
VDD	Y20	VDD	AE27	VDDIO	W4
VDD	Y22	VDD	AG19	VDDIO	Y6
VDD	Y24	VDD	AH24	VDDIO	AA4
VDD	AA9	VDDA1	AH25	VDDIO	AA7
VDD	AA11	VDDA2	AJ25	VDDIO	AB6
VDD	AA13	VDDIO	D5	VDDIO	AB8
VDD	AA15	VDDIO	D7	VDDIO	AC4
VDD	AA17	VDDIO	D9	VDDIO	AC7
VDD	AA19	VDDIO	D11	VDDIO	AC9
VDD	AA21	VDDIO	D13	VDDIO	AD6
VDD	AA23	VDDIO	D15	VDDIO	AD8
VDD	AA28	VDDIO	E4	VDDIO	AD10
VDD	AB10	VDDIO	F6	VDDIO	AD12
VDD	AB12	VDDIO	F8	VDDIO	AD14
VDD	AB14	VDDIO	F10	VDDIO	AD16
VDD	AB16	VDDIO	F12	VDDIO	AE4
VDD	AB18	VDDIO	F14	VDDIO	AF11
VDD	AB20	VDDIO	F16	VDDIO	AF13
VDD	AB22	VDDIO	G4	VDDIO	AF5
VDD	AB24	VDDIO	G7	VDDIO	AF7
VDD	AB26	VDDIO	G9	VDDIO	AF9
VDD	AC11	VDDIO	H6	VDDIOFB_H	AE12
VDD	AC13	VDDIO	H8	VDDIOFB_L	AF12
VDD	AC15	VDDIO	J4	VDDIO_SENSE	AE11
VDD	AC17	VDDIO	J7	VID[0]	AE15
VDD	AC19	VDDIO	K6	VID[1]	AF15
VDD	AC21	VDDIO	L4	VID[2]	AG14
VDD	AC23	VDDIO	M6	VID[3]	AF14
VDD	AD18	VDDIO	N4	VID[4]	AG13

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
VLDT0_A	B27	VSS	D26	VSS	H17
VLDT0_A	B29	VSS	D28	VSS	H19
VLDT0_A	C26	VSS	E15	VSS	H21
VLDT0_A	C28	VSS	E16	VSS	H23
VLDT0_A	D25	VSS	E18	VSS	H26
VLDT0_A	D27	VSS	E22	VSS	J6
VLDT0_A	D29	VSS	E24	VSS	J8
VLDT0_B	AF25	VSS	F2	VSS	J10
VLDT0_B	AE28	VSS	F7	VSS	J12
VLDT0_B	AF29	VSS	F9	VSS	J14
VLDT0_B	AG26	VSS	F11	VSS	J16
VLDT0_B	AG28	VSS	F13	VSS	J18
VLDT0_B	AH27	VSS	F15	VSS	J20
VLDT0_B	AH29	VSS	F17	VSS	J22
VSS	B2	VSS	F19	VSS	J24
VSS	B4	VSS	F21	VSS	K2
VSS	B6	VSS	F23	VSS	K7
VSS	B8	VSS	G6	VSS	K9
VSS	B10	VSS	G8	VSS	K11
VSS	B12	VSS	G10	VSS	K13
VSS	B14	VSS	G12	VSS	K15
VSS	B16	VSS	G14	VSS	K17
VSS	B22	VSS	G16	VSS	K19
VSS	B25	VSS	G18	VSS	K21
VSS	B26	VSS	G20	VSS	K23
VSS	B28	VSS	G22	VSS	L6
VSS	C25	VSS	G24	VSS	L8
VSS	C27	VSS	G28	VSS	L10
VSS	C29	VSS	H2	VSS	L20
VSS	D2	VSS	H7	VSS	L22
VSS	D16	VSS	H9	VSS	L24
VSS	D19	VSS	H11	VSS	L28
VSS	D21	VSS	H13	VSS	M2
VSS	D23	VSS	H15	VSS	M7

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin	Name	Pin
VSS	M9	VSS	V2	VSS	AB7
VSS	M21	VSS	V7	VSS	AB9
VSS	M23	VSS	V9	VSS	AB11
VSS	M26	VSS	V21	VSS	AB13
VSS	N6	VSS	V23	VSS	AB15
VSS	N8	VSS	W6	VSS	AB17
VSS	N10	VSS	W8	VSS	AB19
VSS	N20	VSS	W10	VSS	AB21
VSS	N22	VSS	W20	VSS	AB23
VSS	N24	VSS	W22	VSS	AC6
VSS	P2	VSS	W24	VSS	AC8
VSS	P7	VSS	W28	VSS	AC10
VSS	P9	VSS	Y2	VSS	AC12
VSS	P21	VSS	Y7	VSS	AC14
VSS	P23	VSS	Y9	VSS	AC16
VSS	R6	VSS	Y11	VSS	AC18
VSS	R8	VSS	Y13	VSS	AC20
VSS	R10	VSS	Y15	VSS	AC22
VSS	R20	VSS	Y17	VSS	AC24
VSS	R22	VSS	Y19	VSS	AC28
VSS	R24	VSS	Y21	VSS	AD2
VSS	R28	VSS	Y23	VSS	AD7
VSS	T2	VSS	Y26	VSS	AD9
VSS	T7	VSS	AA6	VSS	AD11
VSS	T9	VSS	AA8	VSS	AD13
VSS	T21	VSS	AA10	VSS	AD15
VSS	T23	VSS	AA12	VSS	AD17
VSS	T26	VSS	AA14	VSS	AD19
VSS	U6	VSS	AA16	VSS	AD21
VSS	U8	VSS	AA18	VSS	AD23
VSS	U10	VSS	AA20	VSS	AD26
VSS	U20	VSS	AA22	VSS	AE14
VSS	U22	VSS	AA24	VSS	AE16
VSS	U24	VSS	AB2	VSS	AE20

Table 4. Pin List by Name (Continued)

Name	Pin	Name	Pin
VSS	AE29	VTT_B	AF16
VSS	AF2	VTT_B	AG15
VSS	AF17	VTT_B	AG16
VSS	AF19	VTT_B	AH16
VSS	AF26	VTT_B	AJ17
VSS	AF28	VTT_SENSE	AE13
VSS	AG20		
VSS	AG21		
VSS	AG22		
VSS	AG23		
VSS	AG24		
VSS	AG25		
VSS	AG27		
VSS	AG29		
VSS	AH2		
VSS	AH4		
VSS	AH6		
VSS	AH8		
VSS	AH10		
VSS	AH12		
VSS	AH14		
VSS	AH20		
VSS	AH22		
VSS	AH26		
VSS	AH28		
VSS	AJ20		
VSS	AJ22		
VSS	AJ24		
VSS	AJ26		
VTT_A	A18		
VTT_A	B17		
VTT_A	C16		
VTT_A	C17		
VTT_A	D17		

6 Pin Descriptions

Table 5 describes the terms used in the pin description tables found in this chapter. The pins are organized within the following functional groups:

- HyperTransport™ technology interface
- DDR SDRAM memory interface
- Miscellaneous pins, including clock, JTAG, and debug pins

All pins are described in the tables beginning on page 35.

Table 5. Pin Description Table Definitions

Pin Types		Applicable Section in Electrical Chapter
I-HT	Input, HyperTransport™ Technology, Differential	"HyperTransport™ Technology Interface" on page 42
O-HT	Output, HyperTransport Technology, Differential	"HyperTransport™ Technology Interface" on page 42
B-IOS	Bidirectional, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 45
I-IOS	Input, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 45
I-IOD	Input, VDDIO[1], Differential	"Clock Pins" on page 57
O-IOD	Output, VDDIO[1], Differential	"Clock Pins" on page 57
O-IOS	Output, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 45
O-IO-OD	Output, VDDIO[1], Open Drain	"DDR SDRAM and Miscellaneous Pins" on page 45
A	Analog	"Power Supplies" on page 65
S	Supply Voltage	"Power Supplies" on page 65
VREF	Voltage Reference	"DDR SDRAM and Miscellaneous Pins" on page 45

Notes:

1. *Refer to Table 31, "Combined AC and DC Operating Conditions for Power Supplies," on page 65 for VDDIO voltage specifications.*

6.1 HyperTransport™ Technology Pins

Table 6. HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input[2]
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT[1]
L0_REF0	A	Compensation Resistor to VSS[1]

Notes:

1. *These pins are used in an alternating fashion to compensate R_{TT} by internal comparison to 3/4 VLDT and 1/4 VLDT and compensate R_{ON} by comparison to each other around 1/2 VLDT. For proper resistor value, see the* AMD Athlon™ 64 Processor Motherboard Design Guide, *order# 24665*.
2. *The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and the complement is pulled Low. Refer to the* AMD Athlon™ 64 Processor Motherboard Design Guide, *order# 24665, for details.*

6.2 DDR SDRAM Memory Interface Pins

Table 7. DDR SDRAM Memory Interface Pin Descriptions

Signal Name	Type	Description
MEMCLK_H/L[7]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[6]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 1 for unbuffered DIMMs.[1]
MEMCLK_H/L[5]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.[1]
MEMCLK_H/L[4]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 1 for unbuffered DIMMs.[1]
MEMCLK_H/L[3]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.[1]
MEMCLK_H/L[2]	O-IOD	Differential DDRS DRAM clock to DIMM 2 for registered DIMMs.[1]
MEMCLK_H/L[1]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.[1]
MEMCLK_H/L[0]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 0 for unbuffered DIMMs, or DIMM 0 for registered DIMMs.[1]
MEMCKEA MEMCKEB	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality.[1]
MEMDQS[17:0]	B-IOS	DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.[1]
MEMDATA[63:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[7:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects[1]
MEMRASA_L MEMRASB_L	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.[1]
MEMCASA_L MEMCASB_L	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.[1]
MEMWEA_L MEMWEB_L	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.[1]
MEMADDA[13:0] MEMADDB[13:0]	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.[1]

Table 7. DDR SDRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description
MEMBANKA[1:0] MEMBANKB[1:0]	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.[1]
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference[1]
MEMZP	A	Compensation Resistor tied to VSS[1]
MEMZN	A	Compensation Resistor tied to 2.5 V[1]

Notes:

1. *For connection details and proper resistor values, see the* AMD Athlon™ 64 Processor Motherboard Design Guide, *order# 24665.*

6.3 Miscellaneous Pins

For connection details for all of the pins in this section, please see the *AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.

Table 8. Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

Table 9. Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125^{o}C.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_A VLDT_B	S	HyperTransport™ I/O ring power supply for side A and side B of the package
VTT_A VTT_B	S	VTT regulator voltage for side A and side B of the die

Table 9. Miscellaneous Pin Descriptions (Continued)

Signal Name	Type	Description
VSS	S	Ground

Table 10. VID[4:0] Encoding

VID[4:0]	VDD	VID[4:0]	VDD	VID[4:0]	VDD	VID[4:0]	VDD
0x00000	1.550 V	0x01000	1.350 V	0x10000	1.150 V	0x11000	0.950 V
0x00001	1.525 V	0x01001	1.325 V	0x10001	1.125 V	0x11001	0.925 V
0x00010	1.500 V	0x01010	1.300 V	0x10010	1.100 V	0x11010	0.900 V
0x00011	1.475 V	0x01011	1.275 V	0x10011	1.075 V	0x11011	0.875 V
0x00100	1.450 V	0x01100	1.250 V	0x10100	1.050 V	0x11100	0.850 V
0x00101	1.425 V	0x01101	1.225 V	0x10101	1.025 V	0x11101	0.825 V
0x00110	1.400 V	0x01110	1.200 V	0x10110	1.000 V	0x11110	0.800 V
0x00111	1.375 V	0x01111	1.175 V	0x10111	0.975 V	0x11111	Off

Table 11. JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Table 12. Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

6.4 Pin States at Reset

The default pin states are listed in Table 13 on page 40. Default pin states are listed for all output and bidirectional pins in the power-on reset state (reset), as well as the ACPI S1 and S3 power-management states.

Table 13. Reset Pin State

Pin Name	Reset State	S1 State	S3 State	Comments
L0_CLKOUT*	T	Z	Z	Tristated in S1 only if programmed to do so.
L0_CTLOUT*	0	Z	Z	Tristated in S1 only if programmed to do so.
L0_CADOUT*	1	Z	Z	Tristated in S1 only if programmed to do so.
MEMCLK*	Z	Z	Z	
MEMDQS*	Z	Z	Z	
MEMCKE*	0	0	0	In S3, MEMCKE* is forced to a logic Low.
MEMDATA*	Z	Z	Z	
MEMCHECK*	Z	Z	Z	
MEMCS_L*	1	Z	Z	
MEMRAS_L	1	Z	Z	
MEMCAS_L	1	Z	Z	
MEMWE_L	1	Z	Z	
MEMADDA*	0	Z	Z	
MEMADDB*	1	Z	Z	MEMADDB* pins are opposite polarity to reduce switching noise.
MEMBANKA*	0	Z	Z	
MEMBANKB*	1	Z	Z	MEMBANKB* pins are opposite polarity to reduce switching noise.
MEMRESET_L	0	0	0	In S3, MEMRESET_L is forced to logic 0.
MEMZN	1	1	1	
MEMZP	0	0	0	
FBCLKOUT*	T	T	Z	
TDO	X	X	Z	
DBRDY	0	0	Z	
VID[4:0]	X	X	X	
THERMTRIP_L	Z	X	Z	

Notes:
For differential inputs, “0” and “1” refer to the high-end differential output. Low-end differential outputs are inverted.Definitions of pin states; X: Either logic 1 or 0, Z: Tristated, T: Toggling between 0 and 1.

7 Electrical Data

7.1 Absolute Maximum Ratings

Stresses greater than those listed in Table 14 may cause permanent damage to the device and motherboard. Systems using this device must be designed to ensure that these parameters are not violated. Violation of these ratings will void the product warranty. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Absolute Maximum Ratings for the AMD Athlon™ 64 Processor

Characteristic	Range
Storage temperature	–55°C to 85°C
VLDT supply voltage relative to VSS	–0.3 V to 1.5 V
VDD supply voltage relative to VSS	–0.3 V to 1.65 V
VTT supply voltage relative to VSS	–0.3 V to 1.65 V
VDDIO supply voltage relative to VSS	–1 V to 2.9 V
VDDA supply voltage relative to VSS	–0.3 V to 3.0 V
MEMVREF input voltage relative to VSS	–1 V to 2.9 V
Input voltage relative to VSS for HyperTransport™ technology interface	–0.3 V to 1.5 V
Differential input voltage for HyperTransport™ technology interface	–1.5 V to 1.5 V
Input voltage relative to VSS for DDR SDRAM memory interface and Miscellaneous pins	–1 V to 2.9V

Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet*, order# 30430, for maximum case temperature specifications.

7.2 HyperTransport™ Technology Interface

7.2.1 Operating Conditions

Table 15. DC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output differential voltage	mV	495	600	715	1, 2
V_{OCM}	Output common mode voltage	mV	495	600	715	1, 2
V_{ID}	Input differential voltage	mV	200	600	1000	1, 2
V_{ICM}	Input common mode voltage	mV	440	600	780	1, 2
DeltaV_{OD}	Change in V_{OD} from 0 to 1 state	mV	–15	0	15	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 state	mV	–15	0	15	1
DeltaV_{ID}	Change in V_{ID} from 0 to 1 state	mV	–15	0	15	1
DeltaV_{ICM}	Change in V_{ICM} from 0 to 1 state	mV	–15	0	15	1
I_l	Input leakage current	mA	–1		1	
I_{OZ}	Output tristate leakage current	mA	–1		1	
R_{ON}	Output driver impedance	ohm	45	50	55	
DeltaR_{ON}	Change in R_{ON} driving 0=>1 or 1=>0	%	–2.5	0	2.5	
R_{TT}	Input differential impedance	ohm	90	100	110	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured at <100 MHz, considered slow enough to attain both 0 and 1 logic state voltage levels without AC transients on signals and supplies.*

Table 16. AC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output differential voltage	mV	400		820	1
V_{OCM}	Output common mode voltage	mV	440		780	1
V_{ID}	Input differential voltage	mV	300		900	1
V_{ICM}	Input common mode voltage	mV	385		845	1
DeltaV_{OD}	Change in V_{OD} from 0 to 1 state	mV	–75		75	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 state	mV	–50		50	1
DeltaV_{ID}	Change in V_{ID} from 0 to 1 state	mV	–125		125	1
DeltaV_{ICM}	Change in V_{ICM} from 0 to 1 state	mV	–100		100	1
T_{RISE}	Input rising edge rate	V/ns	1		4	1, 2
T_{FALL}	Input falling edge rate	V/ns	1		4	1, 2
C_{IN}	Input pad capacitance	pF			2	
C_{OUT}	Output pad capacitance	pF			3	
C_{DELTA}	C_{IN} pad capacitance range across group	pF			0.5	
T_{CADV}	Output CAD valid	pS	166		459	3
TPHERR	Accumulated phase error, CLKIN_H/L to L0_CLKOUT_H/L[1:0]	pS	0		5000	
PLL_Lock	PLL lock time during FID_Change	µs			2	
T_{SU}	Device setup time	pS			110	3, 4
T_{HLD}	Device hold time	pS			110	3, 4
R_{TT}	Input differential impedance	ohm	90	100	110	
R_{ON}	Output impedance	ohm	45	50	55	
DeltaR_{ON}	Change in R_{ON} driving 0=>1 or 1=>0	%	–2.5		2.5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured in a differential fashion relative to the complement signal.*
3. *Measured from crossing points of differential pairs.*
4. *Input setup and hold times are measured from the crossing point of CAD versus the crossing point of CLK, effectively including the edge time to achieve VID min AC.*

7.2.2 Reference Information

Table 17. Internal Termination for HyperTransport™ Technology Interface

Pin	Internal Termination	Value	Tolerance
L0_CADIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L0_CTLIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L0_CLKIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%

7.3 DDR SDRAM and Miscellaneous Pins

This section includes electrical specifications for all DDR SDRAM pins described in "DDR SDRAM Memory Interface Pins" on page 36, and the **THERMTRIP_L**, **RESET_L**, **LDTSTOP_L**, **PWROK**, **VID[4:0]**, **TCK**, **TMS**, **TRST_L**, **TDI**, **TDO**, **DBREQ_L**, and **DBRDY** pins described in "Miscellaneous Pins" on page 38.

7.3.1 Operating Conditions

Table 18. DC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	$0.49*V_{DDIO\_dc}$ Min	$0.5*V_{DDIO\_dc}$	$0.51*V_{DDIO\_dc}$ Max	1, 12
I_l	Input leakage current Any input: $0 \le V_{IN} \le V_{DDIO}$ V (All other pins not under test = 0V)	mA	-1		1	
I_{oz}	Output leakage current Any output: $0 \le V_{OUT} \le V_{DDIO}$ V	mA	-1		1	
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.15	-	-	2
V_{IL}	Input low voltage (logic 0)	V	-	-	V_{ref} - 0.15	2
V_{OH}	Output high voltage (logic 1) (for VID[4:0])	V	2.0			
	Output high voltage (logic 1) (for all other pins)	V	1.8			
V_{OL}	Output low voltage (logic 0)	V			0.65	
I_{OH}	Output levels -Output high current ($V_{OUT}= V_{DDIO}/2$)	mA	-25	-28	-33	3
I_{OL}	Output levels - Output low current ($V_{OUT}=V_{DDIO}/2$)	mA	25	28	32	3
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.2	1.3	1.4	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-100	-	100	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	1.1	1.25	1.4	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-100	-	100	7

Notes:
The notes for Table 18 through Table 21 appear on page 48.

Table 19. AC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	V_{ref}(DC) - 2%		V_{ref}(DC) + 2%	1
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.35	-		2
V_{IL}	Input low voltage (logic 0)	V		-	V_{ref} - 0.35	2
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.0	1.3	1.6	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-150	-	150	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	0.9	1.25	1.6	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-200	-	200	7

Table 20. Input Capacitance

Symbol	Parameters	Unit	Min	Typ	Max	Notes
C_{in}	Input capacitance (DQ & DQS)	pF	3.0	3.5	4.0	
ΔC	Delta Input capacitance	pF	-	-	0.4	8

Table 21. Slew Rate of DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
S_{OUT}	Output slew rate (pullup and pull-down)	V/ns	2	3	4	9
S_{OUT_Ratio}	Output slew rate ratio between pullup and pulldown		0.75	1	1.25	10
S_{in}	Input slew rate	V/ns	0.5		4	11

1. *V_{ref} is expected to be equal to 0.5*V_{DDIO} and to track variations in the DC level of the same. Peak to peak noise on V_{ref} may not exceed $\pm$ 2% of the DC value.*
2. *The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. The receiver effectively switches to the new logic state when receiver input crosses the AC level. The new logic state is maintained as long as the input stays beyond the DC threshold.*
3. *With compensation the granularity between NMOS current and PMOS current cannot exceed 3mA. The range is 6mA due to 10% variation.*
4. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
5. *ΔV_{OD} is the change in magnitude between the differential output voltage while driving a logic 0 and while driving a logic 1.*
6. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage magnitude relative to ground under DC or AC conditions.*
7. *ΔV_{OCM} is the change in magnitude between the output common mode voltage while driving a logic 0 and while driving a logic 1.*
8. *ΔC means the difference in capacitance between any MEMDATA/MEMDQS pin to any other MEMDATA/MEMDQS pin.*
9. *Pullup and pulldown slew rate is measured into R_{TT} (50 Ohms) to V_{TT} as shown in Figure 4. The slew rate is measured between $V_{ref} \pm$ 300 mV. It is designed for any pattern of data, including all outputs switching and only one output switching.*
10. *The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.*
11. *The slew rate is measured at the CPU pin between $V_{ref} \pm$ 150 mV. Minimum and maximum input slew rate specification is set based on DRAM output slew rate specification.*
12. *VDDIO_dc is defined in Table 31 on page 65.*

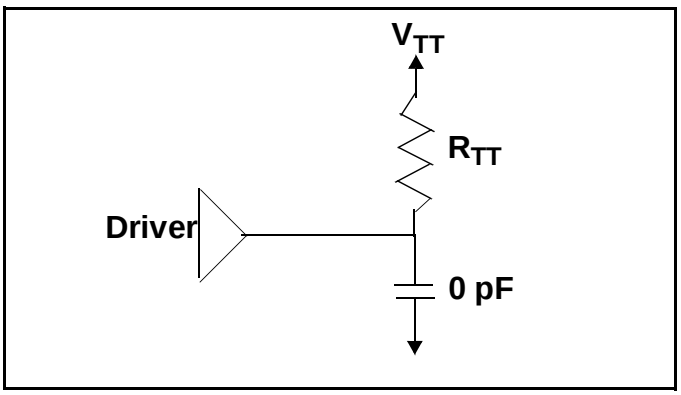


Figure 4. Slew Rate Measurement Example

Table 22. Package Routing Skew

Routing Measurement	Skew (ps)
Any MEMCLK clock pair to any other MEMCLK clock pair	± 100
Any MEMCLK pair to any MEMDQS pair	± 100
Any MEMDQS pair to any MEMDATA associated within pair	± 75
Any MEMCLK pair to any MEMADD/CMD	± 100
Pad skew	± 250

7.3.2 AC Operating Characteristics

Table 23. Electrical AC Timing Characteristics for DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
tCK	MEMCLK cycle time	ps	5000	-	10000	16
tCH	MEMCLK high pulse width	ps	0.45*tCK	-	0.55*tCK	
tCL	MEMCLK low pulse width	ps	0.45*tCK	-	0.55*tCK	
tCKS	MEMCLK output skew	ps	-350	-	350	1,2,3
tDQSH	MEMDQS high pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQSL	MEMDQS low pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQS	MEMCLK to MEMDQS	ps	-350	-	350	1,4,5
tDSS	MEMDQS falling edge to MEM-CLK rising edge	ps	0.45*tCK - 350	-	-	1,6,7
tDSH	MEMCLK rising edge to MEM-DQS falling edge	ps	0.45*tCK - 350	-	-	1,6,7
tDQSQV	MEMDQS to MEMDATA shift (when data becomes valid)	ps	-{0.5* tDQSHmax - [638]}	-	-{0.5* tDQSHmin + [638]}	1,8,9
tDQSQIV	MEMDQS to MEMDATA shift (when data becomes invalid)	ps	{0.5*tDQSH-min - [638]}	-	{0.5* tDQSHmax + [638]}	1,8,9
t1	MEMADD/CMD to MEMCLK (unbuffered DIMM environment - MEMADD/CMD are launched 3/4 clock early)	ps	- 663	-	663	1,10,11
t2	MEMADD/CMD to MEMCLK (Registered DIMM environment - MEMADD/CMD are launched 1/2 clock early)	ps	- 350	-	350	1,10,12
t3	MEMDATA edge arrival relative to MEMDQS	ps	-{tCK/4 - [350+0.2* (tCK/4)]}	-	tCK/4 - [350+0.2* (tCK/4)]	13,14,15

1. *Write cycle timing parameter*
2. *The skew consists of pad output skew (± 250ps) and package routing skew between any two clock pairs (± 100ps).*
3. *tCKS timing parameter, refer to Figure 5 on page 52.*
4. *The timing consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps).*
5. *tDQS timing parameter, refer to Figure 6 on page 52.*

6. *The skew consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps). Minimum DQS pulse width is 45% of MEMCLK.*
7. *tDSS, tDSH timing parameters, refer to Figure 7 on page 53.*
8. *During write, DQ signals are driven quarter clock earlier such that DQS is placed in the center of data eye window. The skew consists of pad output skew (± 250ps), package routing skew between any DQS signals and it's associated DQ signals (± 75ps) and maximum clock granularity (± 312.5 ps).*
9. *tDQSQV and tDQSQIV timing parameters apply only within DQS and its associated DQ signals. Refer to Figure 8 on page 54.*
10. *The skew consists of pad output skew (± 250 ps) and package routing skew (± 100 ps) between any MEMCLK pair to any MEMADD/CMD signal. Maximum clock granularity skew is 312.5 ps.*
11. *t1 timing parameter, applies to unbuffered DIMM environment only - MEMADD/CMD signals are launched 3/4 clock early. The granularity term is included in this parameter only. Refer to Figure 9 on page 55.*
12. *t2 Timing parameter, applies to registered DIMM Environment Only - MEMADD/CMD signals are launched 1/2 clock cycle early. The granularity term does not apply here. Refer to Figure 10 on page 55.*
13. *Read cycle timing parameter.*
14. *The PDL placement uncertainty is 20%. Package skew between DQS and its associated DQs is 75ps. The sum of setup/hold time & receiver uncertainty is 275ps.*
15. *t3 timing parameter, refer to Figure 11 on page 56.*
16. *The slow operation of 10ns cycle time is specifically included for functional test purpose only. All electrical characterization will be performed at full speed however all functional tests will be performed at 10ns cycle time.*

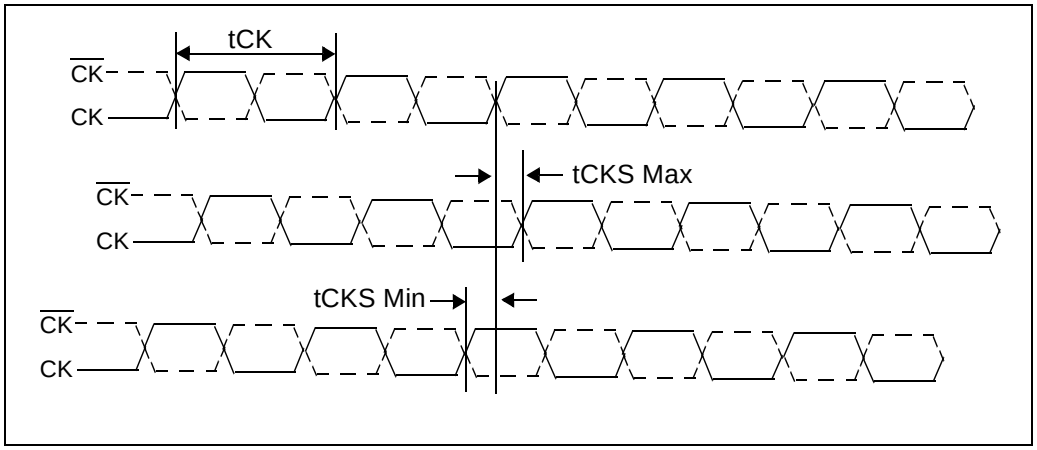


Figure 5. MEMCLK Output Skew

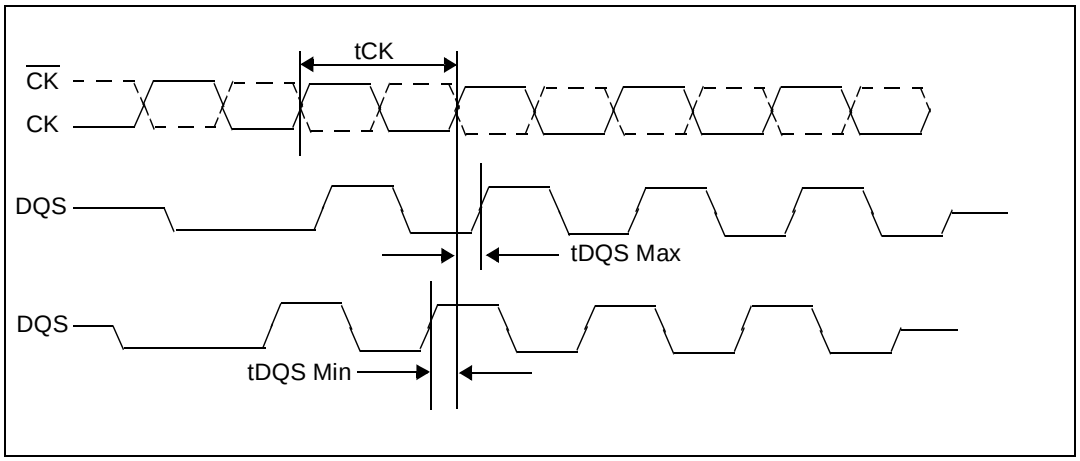


Figure 6. MEMDQS Timing Parameter

t

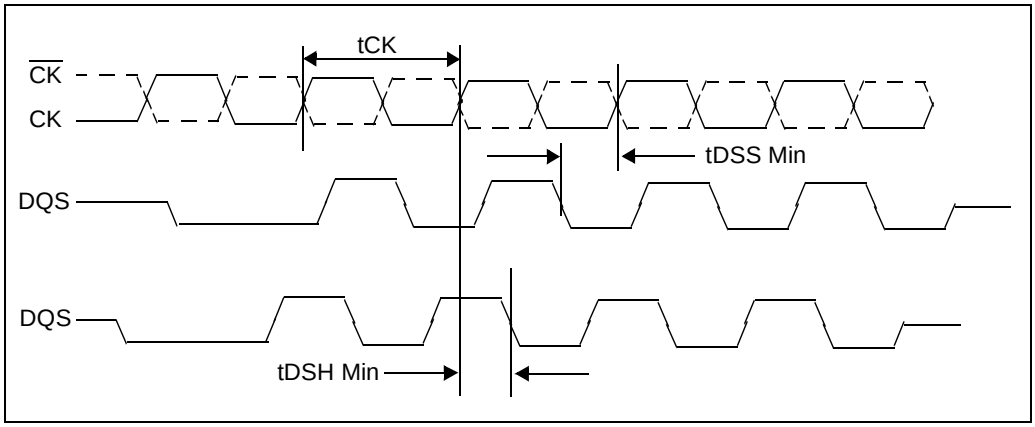


Figure 7. DSS/tDSH Timing Parameters

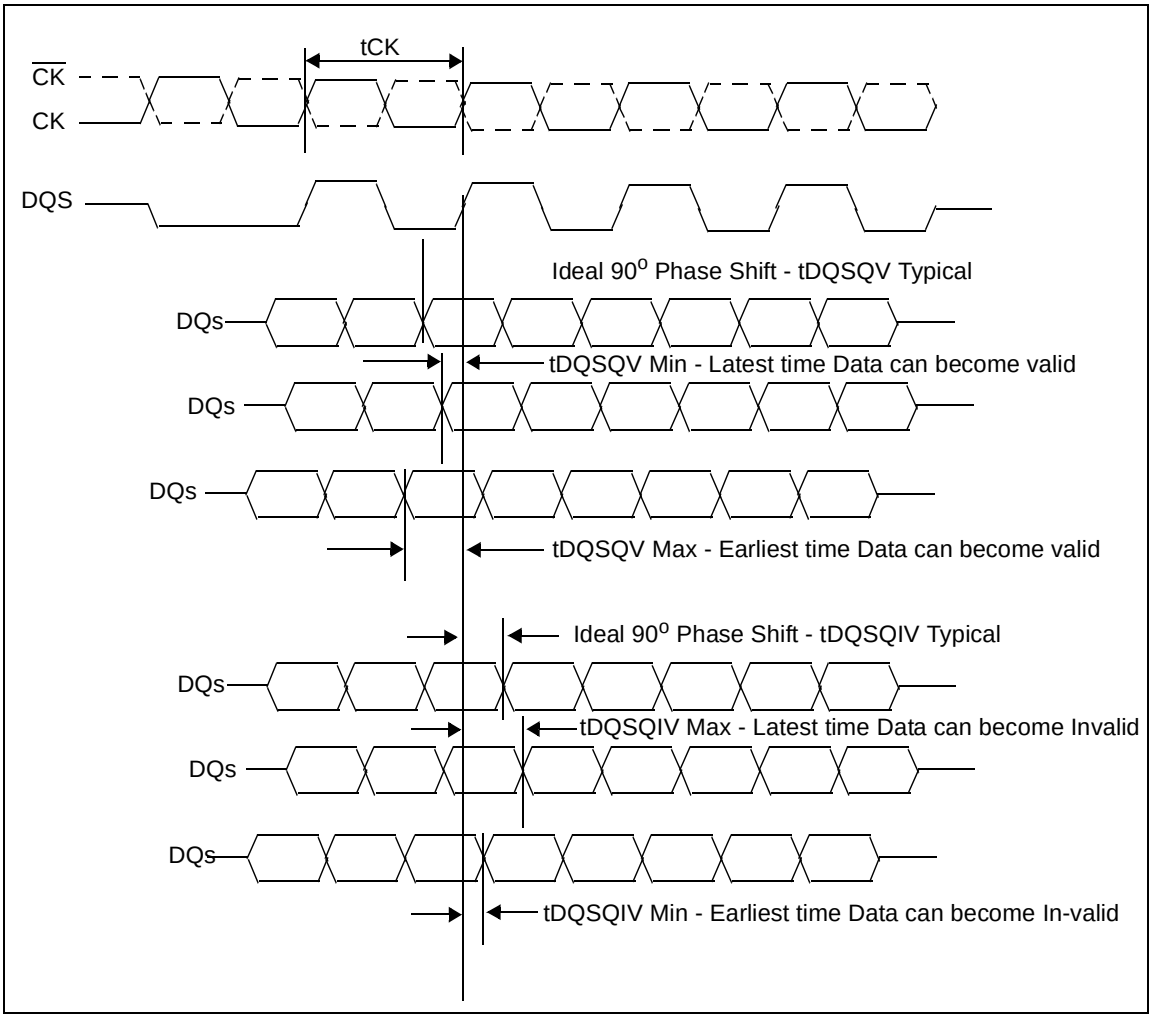


Figure 8. tDQSQV/tDQSQIV Timing Parameters

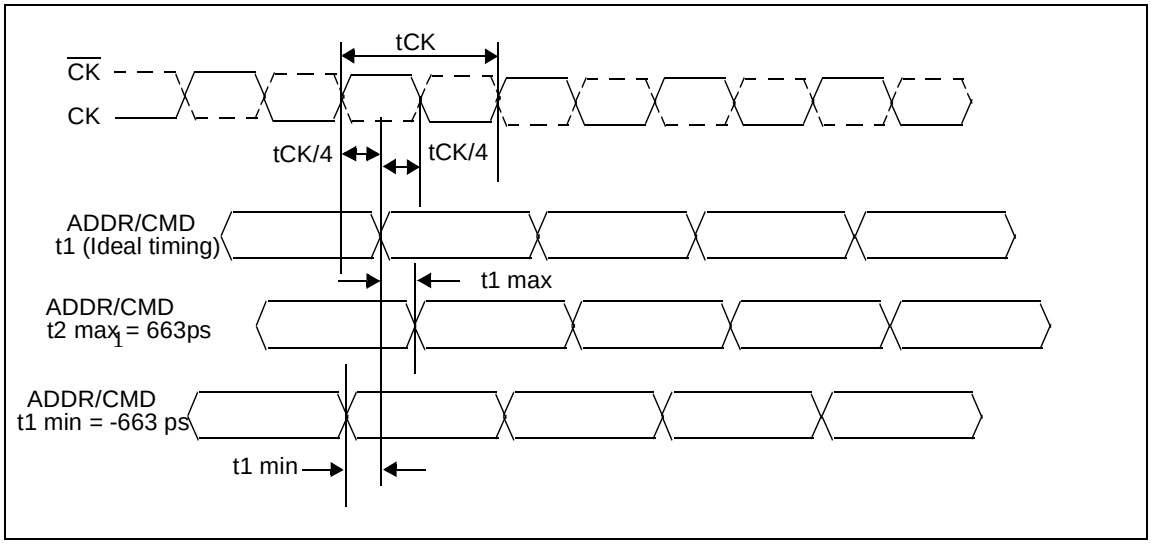


Figure 9. MEMADD/CMD to MEMCLK Timing Parameter (Unbuffered DIMMs)

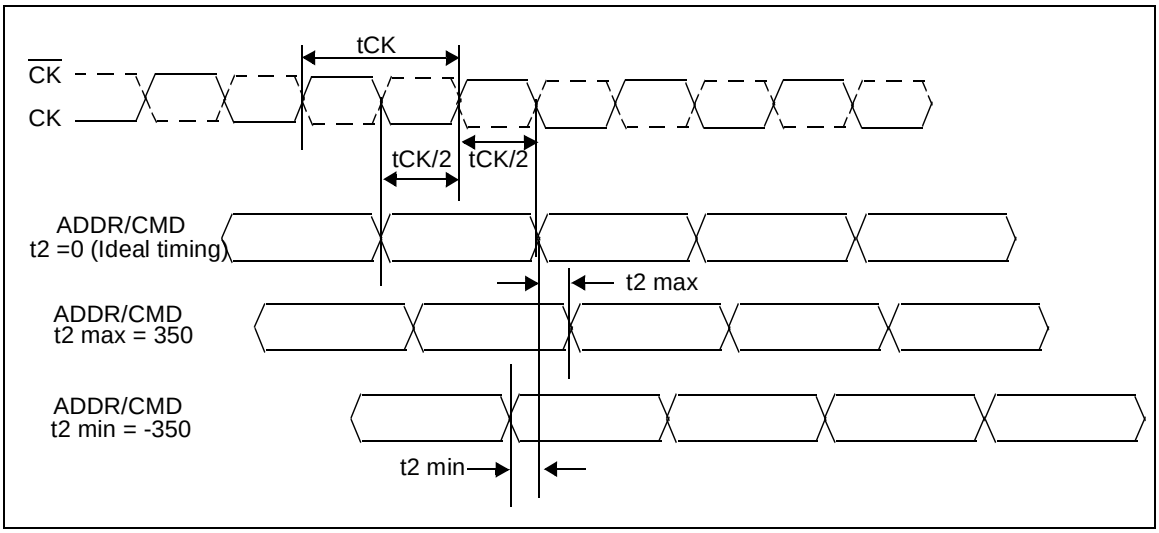


Figure 10. MEMADD/CMD to MEMCLK Timing Parameter (Registered DIMMs)

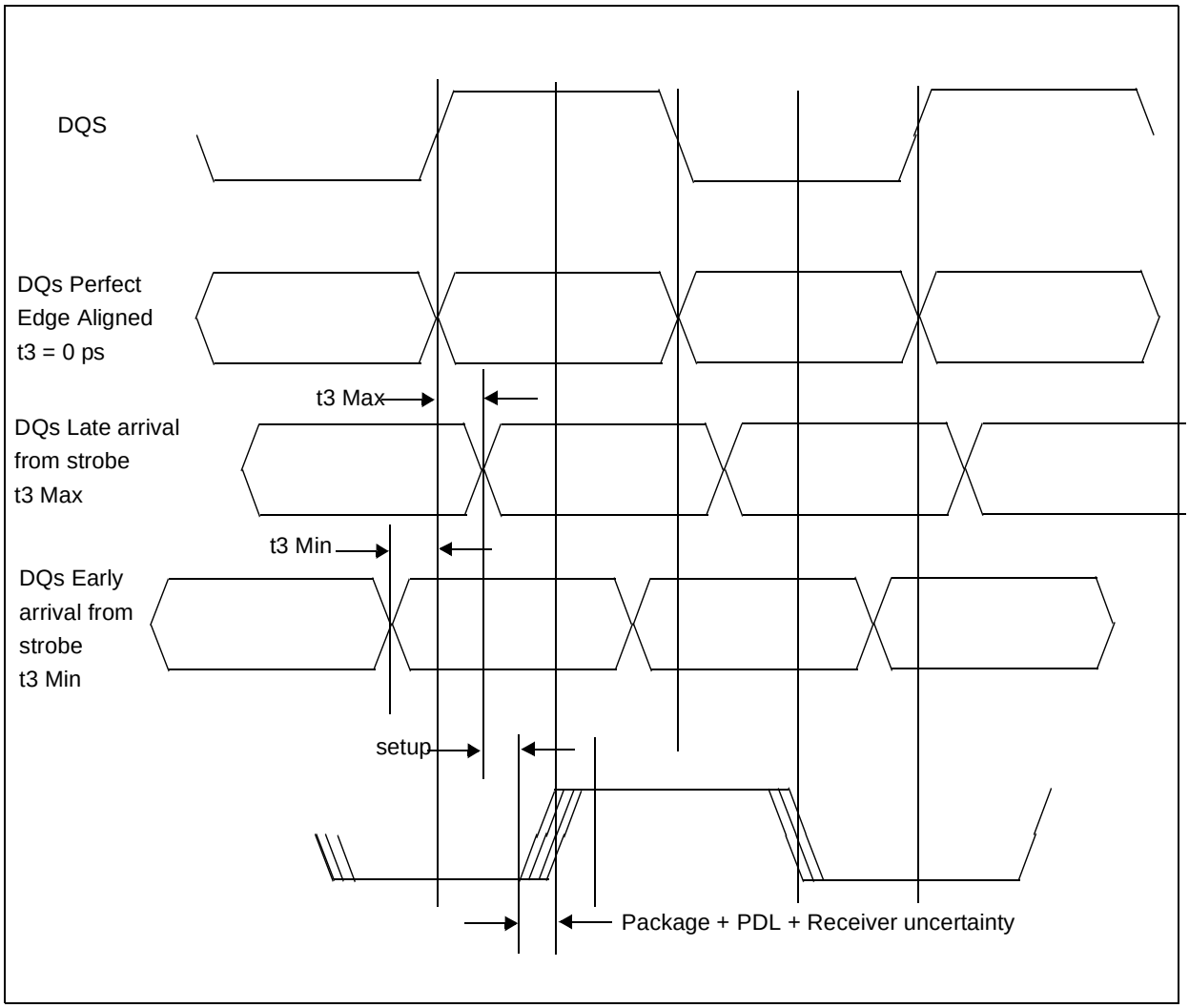


Figure 11. MEMDQS Edge Arrival Relative to DQs

7.4 Clock Pins

7.4.1 Operating Conditions

Table 24. DC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ID}	Differential Input Voltage	mV	300		2400	
DeltaV_{ID}	Change in V_{ID} Magnitude	mV	–50		50	
V_{ICM}	Input Common Mode Voltage	mV	VTT–100	VTT	VTT+100	
DeltaV_{ICM}	Change in V_{ICM} Magnitude	mV	–50		50	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
DeltaV_{OD}	Change in V_{OD} Magnitude	mV	–50		50	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
DeltaV_{OCM}	Change in V_{OCM} Magnitude	mV	–50		50	4

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *DeltaV_{OD} is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *DeltaV_{OCM} is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*

Table 25. AC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameter	Unit	Min	Typ	Max	Notes
F (PLL mode, VDDA=2.5 V)	Input Frequency Range (SSC)	MHz	198.8		200	6
T_{JC}	Jitter, Cycle-to-Cycle	pS	0		200	7
DC	Input Duty Cycle (CLKIN_H/L)	%	30		70	
V_{BIAS}	Input BIAS Voltage Node	mV	VTT	VTT	VTT	
V_{ID}	Differential Input Voltage	mV	400		2300	
DeltaV_{ID}	Change in V_{ID} Magnitude	mV	–150		150	
V_{ICM}	Input Common Mode Voltage	mV	V_{BIAS}–200		V_{BIAS}+200	
DeltaV_{ICM}	Change in V_{ICM} Magnitude	mV	–200		200	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
DeltaV_{OD}	Change in V_{OD} Magnitude	mV	–100		100	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
DeltaV_{OCM}	Change in V_{OCM} Magnitude	mV	–100		100	4
I_F	Input Falling Edge Rate	V/ns	1.2		10	5
I_R	Input Rising Edge Rate	V/ns	1.2		10	5
C_{IN}	Input Capacitance	pF	0		5	

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *Delta V_{OD} is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *Delta V_{OCM} is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*
5. *Measured differentially through the range of VICM – 400 mV to VICM + 400 mV.*
6. *Spread spectrum clocking is limited to –0.5% downspread under normal operation.*
7. *Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.*

7.5 Power-Up Signal Sequencing

Figure 13 on page 61 illustrates the signal sequencing requirements during a cold reset (power-up conditions). The HyperTransport™ link reset sequencing is defined in the *HyperTransport™ I/O Link Specification*.

The following list describes the power-up signal sequencing illustrated in Figure . Note that the numbered items correspond with the numbers in Figure 13.

1. RESET_L must be asserted a minimum of 1 ms prior to the assertion of PWROK, as defined in the *HyperTransport™ I/O Link Specification*. The TMS pin must be asserted a minimum of 10 nS before PWROK assertion and must be held in the High state a minimum of 10 nS after the assertion of PWROK.
2. CLKIN_H/L must be within specification at the time the VDD power supply begins to ramp.
3. PWROK remains deasserted at least 1 ms after both CLKIN_H/L and all voltages to the processor are within specification for operation. The processor determines if there are devices attached to its HyperTransport links 10 µs after the assertion of PWROK.
4. After PWROK assertion the VID[4:0] signals change from the default code (01110b = 1.2 V) to the value programmed during device manufacturing. The PLL begins locking to the frequency programmed during device manufacturing 160 µs after PWROK is asserted.
5. LDTSTOP_L must be deasserted a minimum of 1 µs before the deassertion of RESET_L, as defined by the *HyperTransport™ I/O Link Specification*.
6. The RESET_L signal remains asserted a minimum of 1 ms after PWROK assertion, as defined in the *HyperTransport™ I/O Link Specification*. The clocks from the transmitters of all HyperTransport devices must be stable before RESET_L is deasserted.
7. The MEMCLK_H/L[7:0]signals are stable after BIOS sets the Memory Clock Ratio Valid (MCR) bit in the DRAM Config Upper register.
8. MEMRESET_L is deasserted after BIOS sets the Dram_Init bit in the DRAM Config Lower register. This allows time for the PLL on registered DIMMs to stabilize before the deassertion of the DIMM's reset signal. The delay between these events is described in Figure 12 and Table 26 on page 60.
9. The MEMCKEA/B signals are asserted following the deassertion of MEMRESET_L. The delay between these events is described in Figure 12 and Table 26 on page 60. Note that the MEMCKEA/B delay from MEMRESET_L is different when exiting self-refresh as listed in Table 27 on page 60.

Figure 12. MEMRESET_L and MEMCKEA/B Sequencing

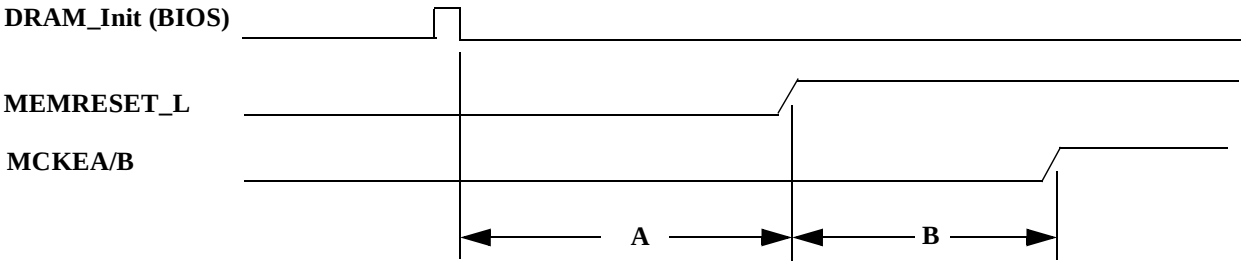


Table 26. MEMRESET_L and MEMCKEA/B Initialization Timing

DRAM Speed	Timing Parameter A	Timing Parameter B
DDR200	163.8µS	491.5µS
DDR266	123.2µS	369.6µS
DDR333	98.7µS	296.1µS
DDR400	81.9µS	245.8µS

Table 27. MEMCKEA/B Delay from MEMRESET_L During Exit from Self-Refresh

DRAM Speed	Unbuffered DIMMs	Registered DIMMs
DDR200	120nS	10.24µS
DDR266	90.2nS	7.6µS
DDR333	72.2nS	6.1µS
DDR400	60nS	5.1µS

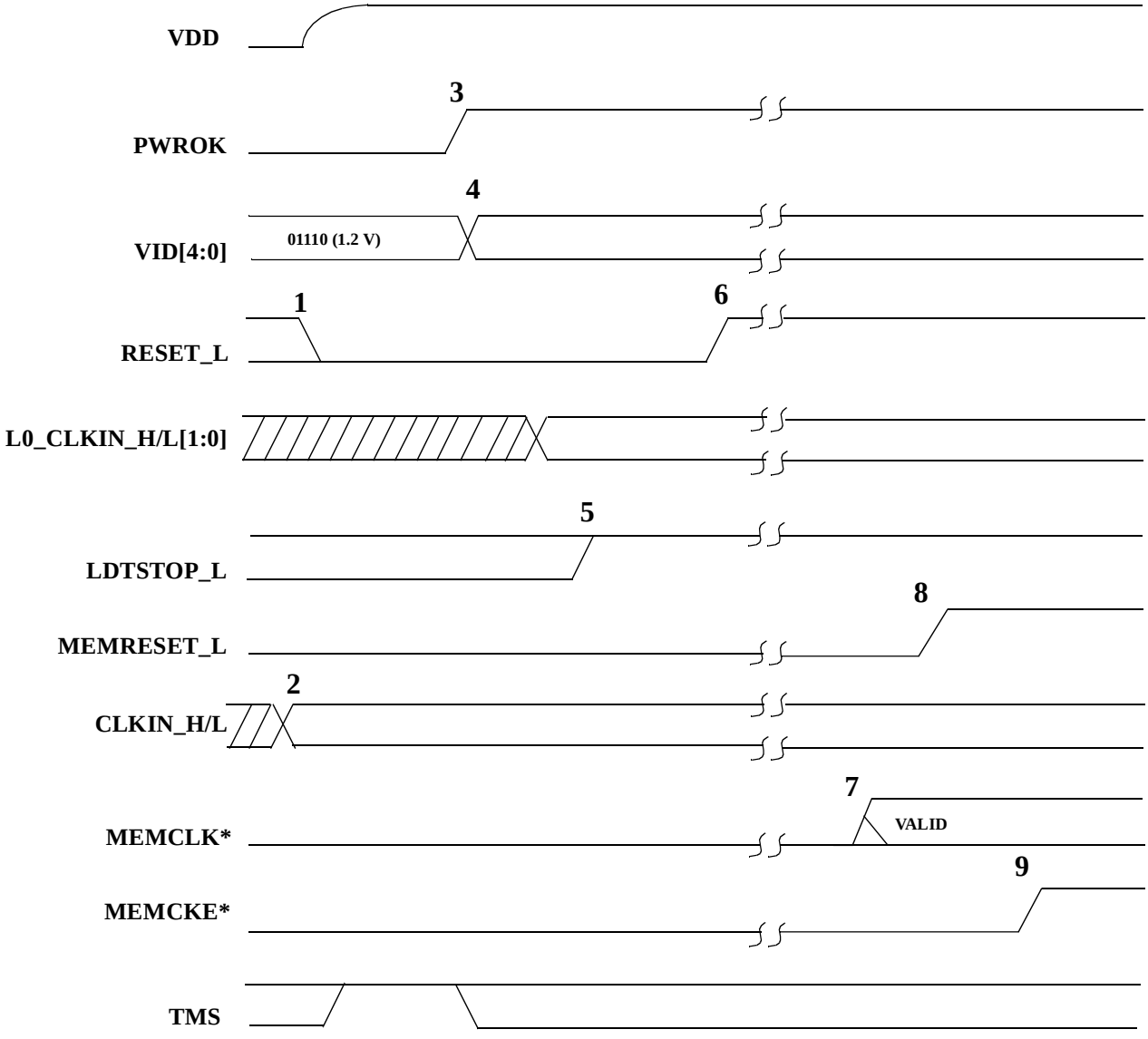


Figure 13. Power-Up Signal Sequencing

7.6 Reference Information

Table 28. Internal Termination for Miscellaneous Pins Interface

Pin	Type[2]	Internal Termination	Value	Tolerance
CLKIN_H/L	I-IOD	None[1]		
FBCLKOUT_H/L	O-IOD	80-ohm differential termination		±50%
RESET_L	I-IOS	None		
PWROK	I-IOS	None		
VID[4:0]	O-IOS	None		
LDTSTOP_L	I-IOS	None		
THERMDA	A	None		
THERMDC	A	None		
THERMTRIP_L	O-IO-OD	None		
COREFB_H/L	A	None		
TCK	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TMS	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TRST_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDI	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDO	O-IOS	Pullup to VDDIO	533 ohms	±50%
DBREQ_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
DBRDY	O-IOS	Pullup to VDDIO	533 ohms	±50%

Notes:

1. *CLKIN_H/L inputs have DC voltage BIAS generating circuits on the inputs. These consist of both a ~250-ohm pullup resistor to VTT on each input and a ~250-ohm series input resistor.*
2. *Refer to“Pin Descriptions” on page 34 for definitions in pin Type column.*
3. *Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used they must not be driven with open-drain outputs or additional termination is required.*

Table 29. External Required Circuits (Pins Not Normally Used in System)

Pin	External Circuit (Non-Operating)[1]
NC_AJ23	Tied to VDDIO_SUS through resistor
NC_AH23	Tied to VSS through resistor
NC_A19	Tied to VDDIO_RUN through resistor
NC_C18	Tied to VDDIO_RUN through resistor
NC_D20	Tied to VSS through resistor
NC_C21	Tied to VSS through resistor
NC_D18	Tied to VSS through resistor
NC_B19	Tied to VSS through resistor
NC_C19	Tied to VSS through resistor

Notes:

1. See the AMD Athlon™ 64 Processor Motherboard Design Guide, *order# 24665, for proper resistor values.*

7.7 Thermal Diode Specifications

An on-die thermal diode is provided as a tool for thermal management. An external sensor is necessary to measure the temperature of the thermal diode.

Thermal solutions should be not designed and validated using the thermal diode. Thermal solutions should be designed and validated against the case temperature specification per the methodology specified in *AMD Athlon™ 64 Processor Thermal Guide*, order# 26633.

Table 30. Thermal Diode Specifications for the AMD Athlon™ 64 Processor

Symbol	Parameter	Units	Min	Typ	Max	Notes
I	Sourcing Currents	µA	5		500	1
T_{Offset}	Temperature Offset	°C	0		52	2, 3, 4, 5

Notes:

1. *The sourcing current should always be used in forward bias.*
2. *The temperature offset is used to normalize the thermal diode measurement to reflect case temperature at the worst case conditions for a part.*
3. *This diode offset supports temperature sensors using two or more sourcing currents only. Single sourcing current implementations are not supported by AMD.*
4. *The temperature offset is unique for each processor and is programmed at the factory. The diode offset value is found in the Thermtrip Status Register described in the* BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, *order# 26094.*
5. T_{Offset} *should be subtracted from the temperature sensor reading. If the temperature sensor has an ideality factor different from 1.008, a small correction to this offset is required. Contact your temperature sensor vendor to determine if additional correction is required.*

7.8 Power Supplies

7.8.1 Operating Conditions

Table 31. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VID_VDD	VID requested VDD supply level	V	See Note 10			5
VDD_dc	VDD supply voltage	V	VID_VDD –50 mV	VID_VDD	VID_VDD +50 mV	
VDD_ac	VDD supply voltage	V	VID_VDD –140 mV		VID_VDD +150 mV	11
VDD_PON	VDD Supply Voltage before PWROK assertion during power-on.	V	1.15	1.20	VDD_max	7
VDDIO_dc	VDDIO supply voltage for DDR 333 and below	V	2.40	2.50	2.60	9
VDDIO_dc	VDDIO supply voltage for DDR 400	V	2.50	2.60	2.65	9
VDDIO_ac	VDDIO supply voltage	V	VDDIO_dc -150 mV		VDDIO_dc +150 mV	8
VLDT	VLDT supply voltage	V	1.14	1.20	1.26	
VTT_dc	VTT supply voltage	V	VDDIO_dc Min/2 - 50 mV	VDDIO_dc Typ/2	VDDIO_dc Max/2 + 50 mV	
VTT_ac		V	VTT_dc - 150 mV		VTT_dc + 150 mV	8
VDDA	VDDA supply voltage	V	2.40	2.50	2.60	
IDD	VDD power supply current	A	See Note 10			
IDDIO1	VDDIO power supply current	A		1.9	2.2	3
IDDIO2	VDDIO power supply current in S3 state	mA			480	
ITT1	VTT power supply current	mA			125	1, 4
ITT2	VTT power supply current in S3 state	mA			125	
ILDT	VLDT power supply current	mA			500	
IDDA	VDDA power supply current	mA			33	
IDDslew1	VDD power supply current change during normal operation	A/µs			$.0583*f^{MHz}$	2, 6
IDDslew2	VDD power supply current change upon reset exit	A/µs			270	2
IDDslew3	VDD power supply current change upon stop grant entry	A/µs	–270			2
IDDslew4	VDD power supply current change upon stop grant exit	A/µs			270	2

Table 31. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
IDDslew5	VDD power supply current change upon non-reset power failure	A/µs	–4.25			2

1. *VTT must both sink and source current.*
2. *Current slew rates are controlled by ramping up or down the core frequency in steps during these sequences to control in-rush currents.*
3. *VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.)*
4. *VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.)*
5. *The processor drives a VID code corresponding to this voltage.*
6. *For example, the IDDslew1 calculation for a 1.2 GHz part is (.0583 x 1200)=69.96 A/µS.*
7. *The processor's VID[4:0] outputs select VID_PON nom before PWROK is asserted. Transients up to VDD_max are allowed.*
8. *VDDIO_ac and VTT_ac parameters are measured +/- 1ns of all data bus bits switching.*
9. *Systems designed to DDR400 power supply parameters will also operate correctly with DDR333 and below.*
10. *Refer to the* AMD Athlon™ 64 Processor Power and Thermal Data Sheet, *order# 30430, for these specifications.*
11. *Transient duration below VDD_dc min is limited to < 5µs. Transient duration above VDD_dc max is limited to < 10% duty cycle. Test by probing differentially at COREFB_H and COREFB_L with 20MHz scope bandwidth limit. Test conditions are while running AMD's MAXPOWER64 utility using AMD thermal approved production grade heat sinks in normal room ambient conditions.*

7.8.2 Thermal Power

Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet*, order# 30430, for thermal power specifications.

7.8.3 Power Supply Relationships

7.8.3.1 Sequencing Relationships

Power supply relationships during power-up, power-down, and entry and exit of any power management state must be controlled in order to avoid damage to the device and help ensure proper operation of the device. Figure 14 shows how these relationships are to be maintained and should be specifically ensured by system power generation and distribution schemes. PWROK must be deasserted as VDD decays during power down.VTT and VDDIO are considered SUSPEND planes (on in both S1(RUN) and S3(SUSPEND) states). VDDA, VDD, and VLDT are considered RUN planes and are powered in the S0 and S1 states only. All power supplies should be turned off during the S4 (SUSPEND to DISK) and S5 (SOFT-OFF) states. VDDIO (RUN) is a power rail used for pull-ups on some processor signals that connect to devices that are powered off during S3, such as THERMTRIP_L.

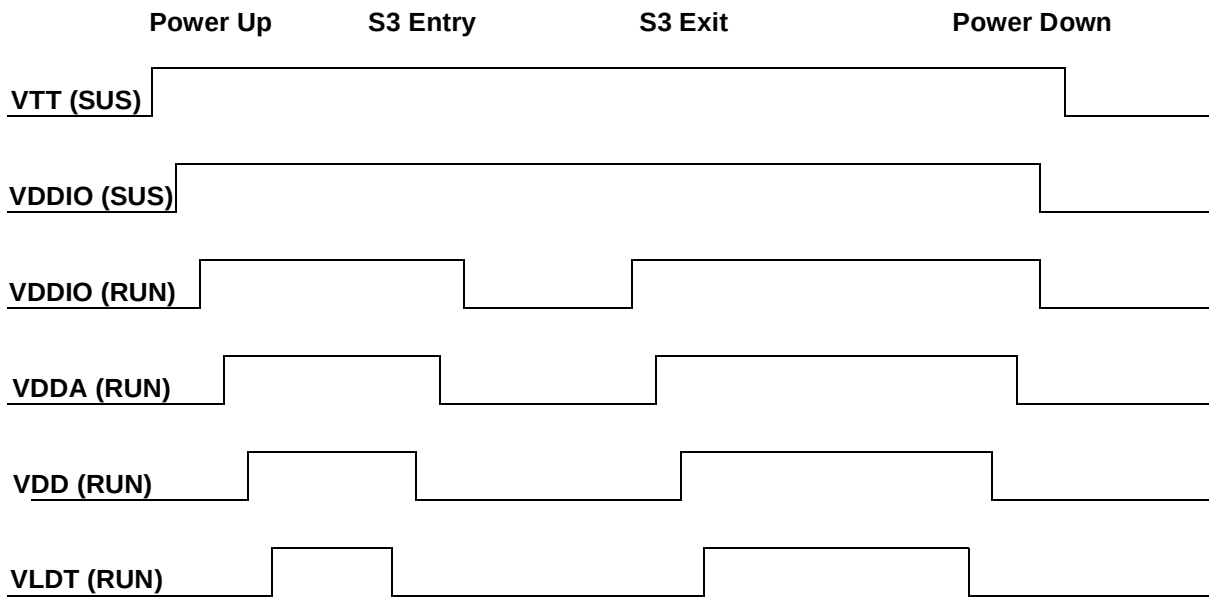


Figure 14. Sequencing Relationships for Power Supplies

Table 32. Sequencing Relationships for Power Supplies

Power Supply Relationship	Unit	Max	Notes
VTT to VDDIO	V	VTT_dc Max	1, 2
VDDIO to VTT	V	VDDIO_dc Max - VTT_dc Typ	1, 3
VDDIO to VDD	V	VDDIO_dc Max	1, 4
VDDA to VDD	V	VDDA Max	1, 5
VDD to VLDT	V	VDD Max	1, 6

Notes:

1. *Sequencing relationships are measured from supply to supply and cover the DC voltage relationships between supplies that must be maintained under all operating conditions including power up, power down, power failure, and power state transitions in order to avoid device or system damage. These relationships can be maintained by propagation of PWRGD signals from one supply rail to the regulator enable of the next supply. The minimum requirements for a proper system implementation are that:*
   - *— VDDIO ramps such that VDDIO/2 <= VTT.*
   - *— VDD ramps such that VDDIO and VDDA are within spec before VDD is enabled.*
   - *— VLDT ramps such that VDD is within spec before VLDT is enabled.*
2. *The VTT to VDDIO relationship allows for VTT to power-up before VDDIO.*
3. *The VDDIO to VTT relationship is critical to avoid overstress of the 2.5-V I/O structures that will occur when VDDIO exceeds VTT by 1.35V during normal operation. VTT must track VDDIO/2 to maintain this specification. During power up and power down VDDIO may exceed VTT by up to 1.5V for no more than 100ms.*
4. *The VDDIO to VDD relationship allows for VDDIO to power-up before VDD.*

5. *The VDDA to VDD relationship allows for VDDA to power-up before VDD. VDDA must power-up before VDD to ensure that internal clock sources are valid before being used and that clock source multiplexors are properly controlled.*
6. *The VDD to VLDT relationship allows for VDD to power-up before VLDT and specifically allows for VDD=VDD_max with VLDT=0 V. VDD must power-up before VLDT to help ensure that PWROK is properly passed from the pins into the VDD power domain such that the deasserted state can be seen in the VLDT power domain.*

7.8.3.2 Sequencing Relationships of Signals to Power Supplies (Stress Conditions)

Once the powerup sequence has been completed and PWROK can be asserted, the sequencing of input signals to the CPU and output signals from the CPU can begin. The requirements from signals to power supplies are summarized by type as follows.

- VDDIO inputs and outputs are allowed to exceed VDDIO by 0.3V and are allowed to be 0.3V below VSS.
- VDDIO inputs are allowed to exceed VTT by VTT_dc Max + 0.3V and are allowed to be 0.3V below VSS.
- VLDT inputs and outputs are allowed to exceed VLDT by 0.3V and are allowed to be 0.3V below VSS.

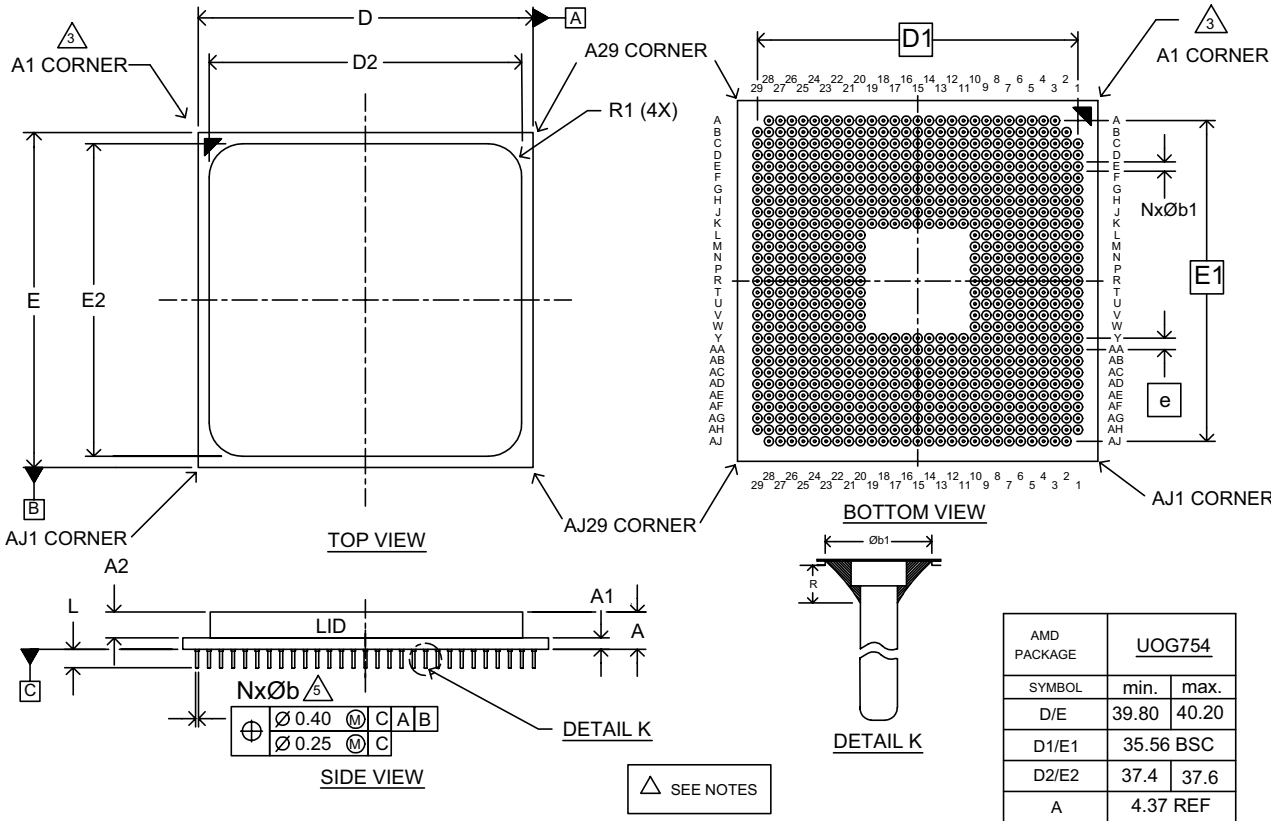
7.8.3.3 Power Failures

The power sequencing relationships defined in sections “Sequencing Relationships” on page 66 and “Sequencing Relationships of Signals to Power Supplies (Stress Conditions)” on page 69 must be guaranteed by the motherboard power supply subsystem in the event of a power failure.

7.8.3.4 Power States

During system power state S3, the RUN supplies (VLDT, VDD, and VDDA) to the CPU are to be turned off. During this operating mode, all internal leakage paths between SUS supplies (VDDIO and VTT) and these powered off planes are disabled. During S0 and S1, all RUN and SUS planes are to be powered on. During S4 and S5, all supplies to the CPU are to be turned off.

8 Package Specifications



AMD PACKAGE	UOG754	
SYMBOL	min.	max.
D/E	39.80	40.20
D1/E1	35.56 BSC	
D2/E2	37.4	37.6
A	4.37 REF	
A1	1.072	1.272
A2	3.06	3.34
e	1.27 BSC	
b	0.275	0.325
b1	0.98	1.08
L	2.03	2.29
M	29	
N	754	
R	0.30 MAX	
R1	4.0 REF	

GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner which consists of a triangle on both sides of the package identifies pin A1 corner and can be used for handling and orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" determines pin matrix size and "N" is number of pins.

Figure 15. Organic Micro Pin Grid Array Package: Top, Side, and Bottom Views (Lidded)